Semiconductors and integrated circuits

Part 6 October 1977

Digital integrated circuits

LOCMOS HE4000B family

SEMICONDUCTORS AND INTEGRATED CIRCUITS

PART 6 — OCTOBER 1977

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DATA HANDBOOK SYSTEM

Our Data Handbook System is a comprehensive source of information on electronic components, sub-assemblies and materials; it is made up of three series of handbooks each comprising several parts.

ELECTRON TUBES	BLUE
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The several parts contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

Where ratings or specifications differ from those published in the preceding edition they are pointed out by arrows. Where application information is given it is advisory and does not form part of the product specification.

If you need confirmation that the published data about any of our products are the latest available, please contact our representative. He is at your service and will be glad to answer your inquiries.

ELECTRON TUBES (BLUE SERIES)

Part 1a	**December 1975**	**ET1a 12-75**	**Transmitting tubes for communication, tubes for r.f. heating** Types PE05/25 to TBW15/25
Part 1b	**August 1977**	**ET1b 08-77**	**Transmitting tubes for communication, tubes for r.f. heating, amplifier circuit assemblies**
Part 2	**May 1976**	**ET2 05-76**	**Microwave products** Communication magnetrons, magnetrons for microwave heating, klystrons, travelling-wave tubes, isolators, circulators, diodes, triodes, T-R switches, microwave semiconductor devices
Part 3	**January 1975**	**ET3 01-75**	**Special Quality tubes, miscellaneous devices**
Part 4	**March 1975**	**ET4 03-75**	**Receiving tubes**
Part 5a	**August 1976**	**ET5a 08-76**	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
Part 5b	**May 1975**	**ET5b 05-75**	**Camera tubes, image intensifier tubes**
Part 6	**January 1977**	**ET6 01-77**	**Products for nuclear technology** Channel electron multipliers, neutron tubes, Geiger-Müller tubes
Part 7a	**March 1977**	**ET7a 03-77**	**Gas-filled tubes** Thyratrons, industrial rectifying tubes, ignitrons, high-voltage rectifying tubes
Part 7b	**March 1977**	**ET7b 03-77**	**Gas-filled tubes** Segment indicator tubes, indicator tubes, switching diodes, dry reed contact units
Part 8	**May 1977**	**ET8 05-77**	**TV picture tubes**
Part 9	**June 1976**	**ET9 06-76**	**Photomultiplier tubes; phototubes**

SEMICONDUCTORS AND INTEGRATED CIRCUITS (RED SERIES)

Part 1a	**March 1976**	**SC1a 03-76**	**Rectifier diodes, thyristors, triacs** Rectifier diodes, voltage regulator diodes (> 1,5 W), transient suppressor diodes, rectifier stacks, thyristors, triacs
Part 1b	**May 1977**	**SC1b 05-77**	**Diodes** Small signal germanium diodes, small signal silicon diodes, special diodes, voltage regulator diodes (< 1,5 W), voltage reference diodes, tuner diodes
Part 2	**December 1975**	**SC2 12-75**	**Low-frequency transistors**
Part 3	**April 1976**	**SC3 04-76**	**High-frequency and switching transistors**
Part 4a	**June 1976**	**SC4a 06-76**	**Special semiconductors** Transmitting transistors, field-effect transistors, dual transistors, microminiature devices for thick and thin-film circuits
Part 4b	**July 1976**	**SC4b 07-76**	**Devices for optoelectronics** Photosensitive diodes and transistors, light emitting diodes, displays, photocouplers, infrared sensitive devices, photoconductive devices
Part 5a	**November 1976**	**SC5a 11-76**	**Professional analogue integrated circuits**
Part 5b	**March 1977**	**SC5b 03-77**	**Consumer integrated circuits** Radio-audio, television
Part 6	**October 1977**	**SC6 10-77**	**Digital integrated circuits** LOCMOS HE4000B family
Signetics integrated circuits 1976			Logic, Memories, Interface, Analogue, Microprocessor, Milrel

COMPONENTS AND MATERIALS (GREEN SERIES)

Part 1	June 1977	CM1 06-77	**Assemblies for industrial use** High noise immunity logic FZ/30-series, counter modules 50-series, NORbits 60-series, 61-series, circuit blocks 90-series, circuit block CSA70(L), PLC modules, input/output devices, hybrid circuits, peripheral devices, ferrite core memory products
Part 2a	October 1977	CM2a 10-77	**Resistors** Fixed resistors, variable resistors, voltage dependent resistors (VDR), light dependent resistors (LDR), negative temperature coefficient thermistors (NTC), positive temperature coefficient thermistors (PTC), test switches
Part 2b	April 1976	CM2b 04-76	**Capacitors** Electrolytic and solid capacitors, paper capacitors and film capacitors, ceramic capacitors, variable capacitors
Part 3	January 1977	CM3 01-77	**Radio, audio, television** FM tuners, loudspeakers, television tuners and aerial input assemblies, components for black and white television, components for colour television
Part 4a	October 1976	CM4a 10-76	**Soft ferrites** Ferrites for radio, audio and television, beads and chokes, Ferroxcube potcores and square cores, Ferroxcube transformer cores
Part 4b	December 1976	CM4b 12-76	**Piezoelectric ceramics, permanent magnet materials**
Part 5	July 1975	CM5 07-75	**Ferrite core memory products** Ferroxcube memory cores, matrix planes and stacks, core memory systems
Part 6	April 1977	CM6 04-77	**Electric motors and accessories** Small synchronous motors, stepper motors, miniature direct current motors
Part 7	September 1971	CM7 09-71	**Circuit blocks** Circuit blocks 100 kHz-series, circuit blocks 1-series, circuit blocks 10-series, circuit blocks for ferrite core memory drive
Part 8	February 1977	CM8 02-77	**Variable mains transformers**
Part 9	March 1976	CM9 03-76	**Piezoelectric quartz devices**
Part 10	November 1975	CM10 11-75	**Connectors**

RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

DEFINITIONS OF TERMS USED

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

ABSOLUTE MAXIMUM RATING SYSTEM

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

DESIGN MAXIMUM RATING SYSTEM

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

DESIGN CENTRE RATING SYSTEM

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices.

The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the stated normal supply voltage.

HE4000B FAMILY — INTRODUCTION

INTRODUCTION TO THE HE4000B FAMILY DATA SHEETS

The LOCMOS HE4000B range is a fully buffered digital integrated circuit family which meets the Jedec-B specification. The members of this family are plug-in replacements for the well-known C-MOS 4000 and 14500 ranges. The HE family has the same advantages as conventional C-MOS circuits, plus the additional LOCMOS advantages.

LOCMOS means: Local Oxidation Complementary MOS.

The main effect of LOCMOS is a considerable reduction in the chip area required for a given function. Also important is the reduction in stray capacitance due to the smaller contact areas - hence the higher switching speed. Another benefit, brought about by the manufacturing process, is the self-alignment of the source and drain diffusions. This means that tolerance margins in the diffusions are unnecessary, thus further reducing the stray capacitances.

Advantages of C-MOS:

- low power dissipation - typically 10 nW per gate (static);
- wide operating supply voltage range;
- wide operating temperature range - −40 to + 85 °C;
- high d.c. fan-out;
- inputs and outputs are protected against electrostatic voltages.

In addition to these, the LOCMOS HE4000B range has:

- buffered outputs on **all** circuits;
- higher speed;
- higher packing density - essential for MSI/LSI;
- excellent noise immunity.

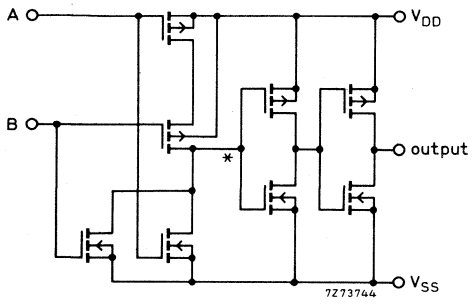
The HE family is designed with standardized output drive characteristics which, combined with relative insensitivity to output capacitance loading, simplify system design.

Note

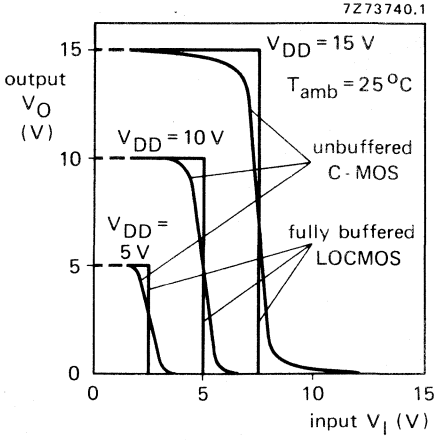
On page 1 of most of the device data sheets are shown a pinning diagram together with a logic symbol. In addition to this logic symbol, a more detailed logic diagram is given, which also shows the buffered outputs.

BUFFERED OUTPUTS

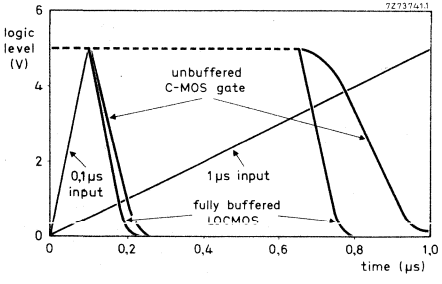
To minimize any pattern sensitivity of propagation delay, and to standardize delay and output drive, all HE family devices have an output buffer stage (see circuit below). Buffering improves the static noise immunity because the increased voltage gain gives nearly ideal transfer characteristics and the low output impedance gives significant improvement of the dynamic noise immunity. Significant pulse shaping is obtained because output transitions are virtually independent of input rise and fall times.

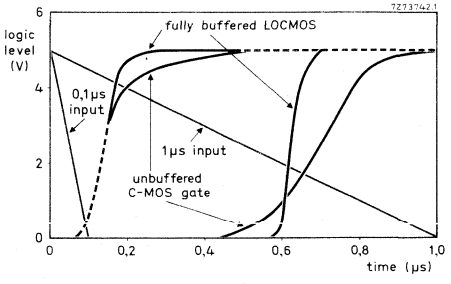


Two-input NOR gate with fully buffered output; a typical LOCMOS circuit.
In an unbuffered device the output would be taken from the point marked *.



Typical transfer characteristic showing improvement in buffered LOCMOS device as compared with unbuffered C-MOS device.





The above two graphs show how the output transitions are independent of input rise time (left-hand graph) and fall time (right-hand graph).

DESIGN CONSIDERATIONS

General

Local Oxidation Complementary MOS digital integrated circuits of SSI and MSI complexity have been hailed as the ideal logic family. A few LOCMOS devices, such as bidirectional analogue switches, exploit the unique feature of C-MOS technology; some take advantage of the smaller device size and higher potential packing density to achieve true LSI complexity, but most of the available LOCMOS elements today are of SSI and MSI complexity and perform logic functions that have been available in TTL for many years. Therefore, it is both helpful and practical to compare the performance of LOCMOS with that of the more familiar TTL (see table below).

LOCMOS speed is about three to six times lower than TTL or low-power Schottky (LS-TTL). Static noise immunity and fan-out are almost ideal, supply voltage is non-critical, and the quiescent power consumption is close to zero - several orders of magnitude lower than for any competing technology.

For dynamic noise immunity, see NOISE IMMUNITY.

	standard TTL	low-power Schottky	4000 LOCMOS 5 V	4000 LOCMOS 10 V	4000 LOCMOS 15 V
propagation delay C_L = 15 pF	10 ns	10 ns	40 ns	20 ns	15 ns
flip-flop clock frequency	35 MHz	45 MHz	8 MHz	16 MHz	20 MHz
quiescent power	10 mW	2 mW	10 nW	10 nW	10 nW
noise immunity	1 V	0,8 V	2,25 V	4,5 V	6,75 V
fan-out	10	10	50 *	50 *	50 *

* Or as determined by permissible propagation delay.

Supply voltage range

LOCMOS is guaranteed to function over the unprecedented range of 3 to 15 V supply voltage. Characteristics are guaranteed for 5, 10 and 15 V operation and can be extrapolated for any voltage in between. Operation below 4,5 V is not very meaningful because of the increase in delay (loss of speed), the increase in output impedance and the loss of noise immunity. Operation above 15 V is not recommended because of high dynamic power consumption and risk of noise spikes on the power supply exceeding the breakdown voltage (typ. $>$ 20 V), causing SCR-latch-up and destroying the device unless the current is externally limited.

The lower limit of power supply voltage, including ripple, is determined by the required noise immunity, propagation delay or interface to TTL. The upper limit of supply voltage, including ripple and transients, is determined by power dissipation or direct interface to other logic. The HEF4049B, HEF4050B and HEF4104B provide level transition between TTL and LOCMOS when LOCMOS supply voltages over 5 V are used.

Low static power consumption combined with wide supply voltage range make LOCMOS the ideal logic family for battery-operated equipment.

Power consumption

Under static conditions, the p-channel and the n-channel transistors are not conducting simultaneously, thus only leakage current flows from the positive (V_{DD}) to the negative (V_{SS}) supply connection. This leakage current is typically 0,5 nA per gate, resulting in a very attractive low power consumption of 2,5 nW per gate (at 5 V).

Whenever a LOCMOS circuit is exercised, when data or clock inputs change, additional power is consumed to charge and discharge capacitances (on-chip parasitic capacitances as well as load capacitances). Moreover, there is a short time during the transition when both the p-channel and n-channel transistors are partially conducting. This dynamic power consumption is obviously proportional to the frequency at which the circuit is exercised, to the load capacitance and to the square of the supply voltage. As shown in Fig.1, the power consumption of a LOCMOS gate exceeds that of a low-power Schottky gate somewhere between 500 kHz and 2 MHz of actual output frequency. Comparing the power consumption of more complex devices (MSI) in various technologies may show a different result.

In any complex design, only a small fraction of the gates actually switch at the full clock frequency, most gates operate at a much lower average rate and therefore consume much less power. A realistic comparison of power consumption between different technologies involves a thorough analysis of the average switching speed of each gate in the circuit.

The maximum values of the quiescent device current (I_{DD}) are given in the Family Specifications, the typical dynamic power dissipation is given in the individual data sheets. The total device power dissipation is the sum of the quiescent and dynamic power dissipation.

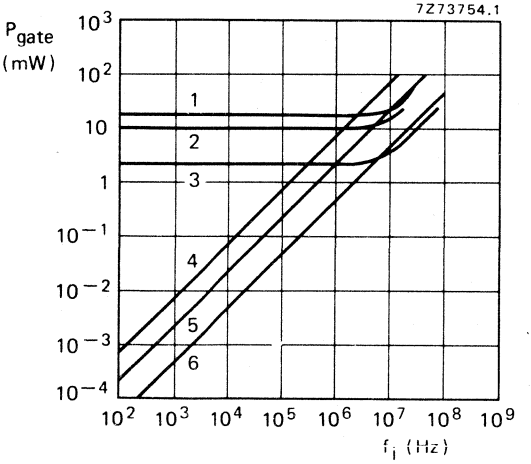


Fig.1 Typical power dissipation per gate as a function of input frequency for several logic families.

1 Schottky TTL
2 Standard TTL
3 Low-power Schottky
4 LOCMOS (V_{DD} = 15 V)
5 LOCMOS (V_{DD} = 10 V)
6 LOCMOS (V_{DD} = 5 V)

Propagation delay

Compared to TTL and LS-TTL, all C-MOS devices are slow and very sensitive to capacitance loading (see Fig.2).

The HE family uses both advanced processing (LOCMOS) and improved circuit design (buffered gates) to achieve propagation delays and output transition times that are superior to any other junction-isolated C-MOS design.

LOCMOS processing achieves lower parasitic capacitances which reduce the on-chip delay and increase the maximum clock frequency of flip-flops, registers and counters. Buffering all outputs, even on gates, results in lower output impedance and thus reduces the effect of capacitive loading.

Propagation delay is affected by three parameters: capacitive loading, supply voltage, and temperature.

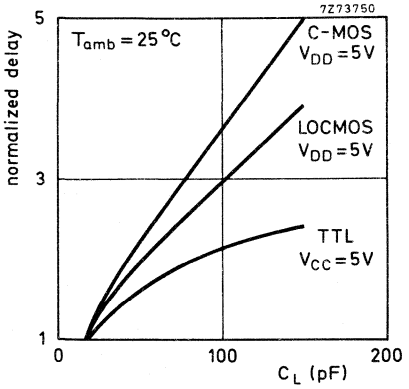


Fig.2 Normalized propagation delay as a function of load capacitance for TTL, C-MOS and LOCMOS.

Capacitive loading effect

Historically, semiconductor manufacturers have always specified the propagation delay at an output load of 15 pF, not because this was considered a representative systems environment, but rather because it was the lowest practical test-jig capacitance. It also generated the most impressive specifications. For example, TTL with an output impedance in the LOW state of typically 25 Ω is little affected by an increase in capacitive loading. LOCMOS, however, with an output impedance of typically 250 Ω (at 5 V) is 10 times more sensitive to capacitive loading. As an example Fig.3 shows the positive and negative-going delays as functions of load capacitance for the HEF4011B and Fig.4 shows the output transition times for standard output stages. For detailed information see Family Specifications and the individual data sheets. It should be noted that most unbuffered gates have an even higher output impedance, a larger dependence on output loading, and do not show the same symmetry.

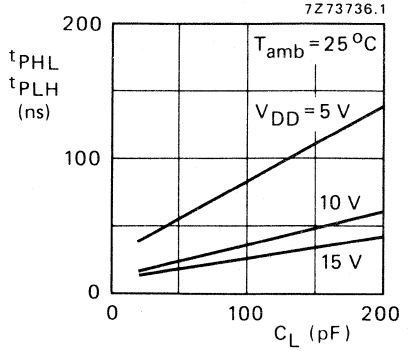


Fig.3 Positive and negative-going propagation delay as functions of load capacitance for the HEF4011B.

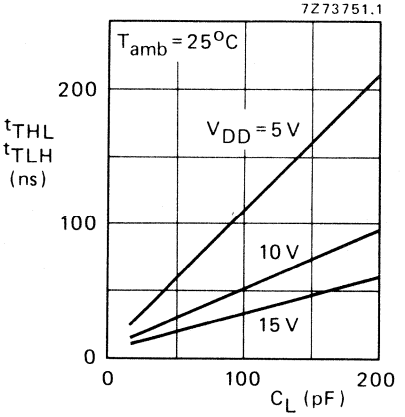


Fig.4 Output transition times as functions of load capacitance.

Supply voltage effect

1. Speed; Fig.5 shows propagation delays as functions of supply voltage. The best choice for slow applications is 5 V. For reasonably fast systems, choose 10 or 12 V. Any application requiring 15 V to achieve short delays and fast operation should be investigated for excessive power dissipation and should be weighed against an LS-TTL approach.
2. Noise immunity; improves with higher supply voltage (see NOISE IMMUNITY).

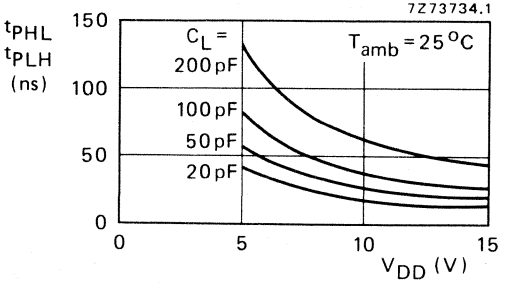


Fig.5 Propagation delays (symmetrical) as functions of power supply voltage for the HEF4011B.

Temperature effect

The temperature dependence of LOCMOS is much simpler than with TTL, where three factors contribute: increase of beta with temperature, increase of resistor value with temperature, and decrease of junction forward voltage drop with increasing temperature. In LOCMOS, essentially only the carrier mobility changes, thus increasing the impedance, and hence the delay, with temperature. For more details see Family Specifications and the individual data sheets, for example see Fig.6.

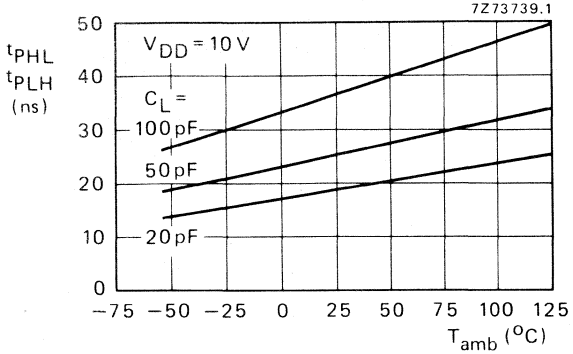


Fig.6 Propagation delays as functions of ambient temperature, with V_{DD} = 10 V for HEF4011B.

Noise immunity

One of the most advertised and also misunderstood C-MOS features is noise immunity. The input threshold of a C-MOS gate is approximately 50% of the supply voltage and the voltage transfer curve is almost ideal. As a result, LOCMOS can claim very good voltage noise immunity, typically 45% of the supply voltage, i.e., 2,25 V in a 5 V system, 4,5 V in a 10 V system and 6,75 V in a 15 V system. Compare this with the TTL transfer curve in Fig.7 and its resultant 1 V noise immunity in a lightly loaded system and only 0,4 V worst case. Fig.8 shows the transfer characteristic between −55 and +125 °C.

Since LOCMOS output impedance, output voltage and input threshold are symmetrical with respect to the supply voltage, the LOW and HIGH level noise immunities are practically equal. Therefore, a LOCMOS system can tolerate ground or V_{DD} drops and noise on these supply lines of more than 1 V, even in a 5 V system. Moreover, the inherent LOCMOS delays act as a noise filter; 10 ns spikes tend to disappear in a chain of LOCMOS gates, but are amplified in a chain of TTL gates. Because of these features, LOCMOS is very popular with designers of industrial control equipment that must operate in an electrically and electromagnetically 'polluted' environment.

Unfortunately these impressive noise margin specifications disregard one important fact: the output impedance of LOCMOS is 3 to 10 times higher than that of TTL. C-MOS interconnections are therefore less 'stiff' and more susceptible to capacitively coupled noise. In terms of such current-injected crosstalk from high noise voltages through small coupling capacitances, the tables on page 8 give a comparison between LOCMOS and TTL/LS-TTL.

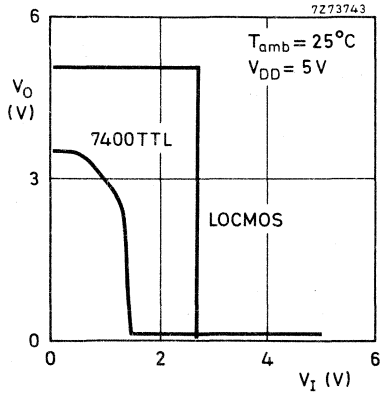


Fig.7 Typical transfer characteristic for TTL and LOCMOS.

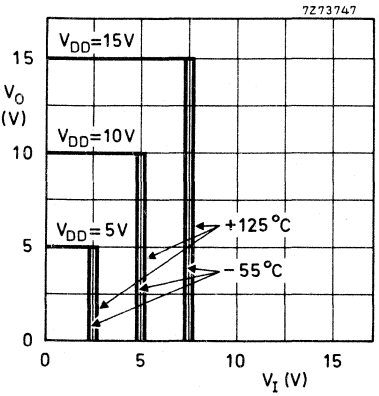


Fig.8 Voltage transfer characteristic over −55 to +125 °C range.

LOCMOS/TTL (normalized to TTL)

V_{DD}	5 V	10 V	15 V
factor	0,5	1	2

LOCMOS/LS-TTL (normalized to LS-TTL)

V_{DD}	5 V	10 V	15 V
factor	1	3	5

From the tables can be seen that LOCMOS operating at V_{DD} = 10 V has a dynamic noise immunity which is comparable with TTL and 3 times as good as LS-TTL.

In terms of voltage injected noise the nearly ideal transfer characteristic and the relatively slow response of LOCMOS circuits make them at least 5 times less sensitive to magnetically coupled noise than TTL/LS-TTL.

Input protection

The gate input to any MOS transistor appears like a small value (< 1 pF), very low leakage (< 1 pA) capacitor. Without special precautions, such inputs could be electrostatically charged to a high voltage, causing a destructive breakdown of the dielectric and permanently damaging the device. Therefore, all LOCMOS inputs are protected by a combination of series resistor and shunt diodes. Different manufacturers have used different approaches; some use a single diode, others use two diodes, and some use a resistor with a parasitic substrate diode.

Each member of the HE family utilizes a series resistor, nominally 400 Ω, and two diodes, one to V_{DD}, and the other to V_{SS} (see Fig.9). The resistor is a polysilicon 'true resistor' without a parasitic substrate diode. This ensures that the input impedance is always at least 400 Ω under all biasing conditions, even when V_{DD} is short-circuited to V_{SS}. A parasitic substrate diode would represent a poorly defined shunt to V_{SS} in this particular case.

The diodes exhibit typical forward voltage drops of 0,9 V at 1 mA and reverse breakdown voltages of 20 V. For certain special applications such as oscillators, the diodes actually conduct during normal operation, in this case the current should be limited to 1 mA. Input currents averaging 10 mA or more may destroy the device.

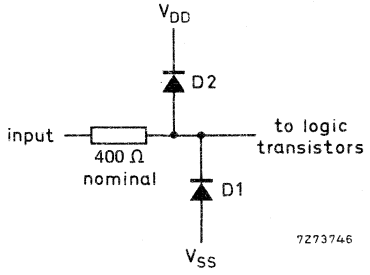


Fig.9 HE family LOCMOS input protection circuit.

Power supply regulation and decoupling

The LOCMOS technology suggests that any supply voltage between 3 and 15 V will do, thus rendering supply voltage regulation unnecessary. However, it must be realized that the supply voltage has influence on the system speed (see page 6), noise immunity (see pages 7 and 8) and dissipation (see page 4).

Any dynamic system generates voltage spikes on the supply line. These spikes influence the noise immunity, they may damage the circuit, or may have a negative influence on proper operation of the circuit. Therefore a matched decoupling of the supply line is necessary. Generally an electrolytic capacitor of 3 μF per 10 devices is sufficient. However, some circuits require special attention:

1. HEF4511B: BCD to 7-segment latch/decoder/driver; an electrolytic capacitor of 3 μF should be added to each device to avoid excessive voltage spikes due to high di/dt.
2. HEF4528B: dual retriggerable/resettable monostable multivibrator; for circuits of this nature it is recommended to use proper decoupling to avoid pulse length variations due to supply line ripple.

FAMILY SPECIFICATIONS

These specifications cover the common electrical characteristics of the entire HE4000B family, unless otherwise specified in the individual device data sheet.

The LOCMOS HE4000B family devices will operate over a recommended V_{DD} power supply range of 3 to 15 V, as referenced to V_{SS} (usually ground). Parametric limits are guaranteed for V_{DD} of 5, 10 and 15 V. Because of the wide operating voltage range, power supply regulation is less critical than with other types of logic. The lower limit of the supply voltage is 3 V, or as determined by required system speed and/or noise immunity or interface to other logic. The recommended upper limit is 15 V or as determined by power dissipation constraints or interface to other logic. Unused inputs must be connected to V_{DD}, V_{SS} or another input. Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage	V_{DD}	−0,5 to +18	V
Voltage on any input	V_I	−0,5 to V_{DD} + 0,5	V *
D.C. current into any input or output	$\pm I_I$	max 10	mA
Power dissipation per package			
for T_{amb} = −40 to +60 °C	P_{tot}	max 400	mW
for T_{amb} = +60 to +85 °C		derate linearly with 8 mW/°C to 200 mW	
Power dissipation per output	P	max 100	mW
Storage temperature	T_{stg}	−65 to +150	°C
Operating ambient temperature	T_{amb}	−40 to +85	°C

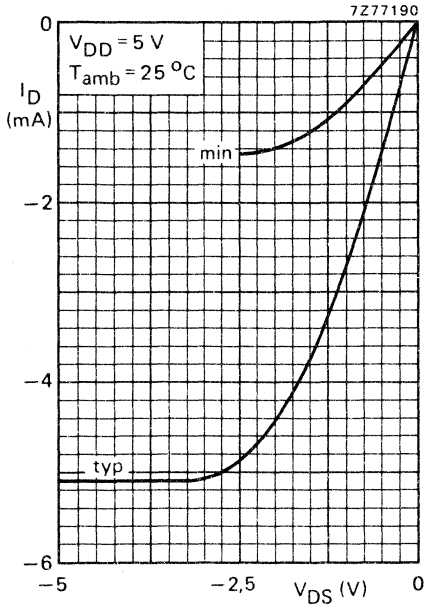
* V_{DD} + 0,5 V should not exceed 18 V.

D.C. CHARACTERISTICS V_{SS} = 0 V

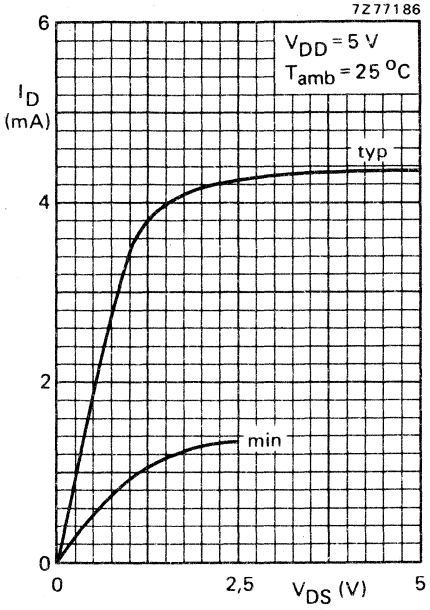
parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			−40		+25		+85			
			min	max	min	max	min	max		
Quiescent device current										
	5		–	1,0	–	1,0	–	7,5	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
gates	10	I_{DD}	–	2,0	–	2,0	–	15,0	μA	
	15		–	4,0	–	4,0	–	30,0	μA	
	5		–	4,0	–	4,0	–	30	μA	
buffers, flip-flops	10	I_{DD}	–	8,0	–	8,0	–	60	μA	
	15		–	16,0	–	16,0	–	120	μA	
	5		–	20	–	20	–	150	μA	
MSI	10	I_{DD}	–	40	–	40	–	300	μA	
	15		–	80	–	80	–	600	μA	
	5		–	0,05	–	0,05	–	0,05	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA
Output voltage LOW	10	V_{OL}	–	0,05	–	0,05	–	0,05	V	
	15		–	0,05	–	0,05	–	0,05	V	
	5		4,95	–	4,95	–	4,95	–	V	$V_I = V_{SS}$ or V_{DD}; $\lvert I_O \rvert < 1$ μA
Output voltage HIGH	10	V_{OH}	9,95	–	9,95	–	9,95	–	V	
	15		14,95	–	14,95	–	14,95	–	V	
	5		–	1,5	–	1,5	–	1,5	V	V_O = 0,5 V or 4,5 V; $\lvert I_O \rvert < 1$ μA
Input voltage LOW	10	V_{IL}	–	3,0	–	3,0	–	3,0	V	V_O = 1,0 V or 9,0 V; $\lvert I_O \rvert < 1$ μA
	15		–	4,0	–	4,0	–	4,0	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1$ μA
	5		3,5	–	3,5	–	3,5	–	V	V_O = 0,5 V or 4,5 V; $\lvert I_O \rvert < 1$ μA
Input voltage HIGH	10	V_{IH}	7,0	–	7,0	–	7,0	–	V	V_O = 1,0 V or 9,0 V; $\lvert I_O \rvert < 1$ μA
	15		11,0	–	11,0	–	11,0	–	V	V_O = 1,5 V or 13,5 V; $\lvert I_O \rvert < 1$ μA

D.C. CHARACTERISTICS (continued) V_{SS} = 0 V

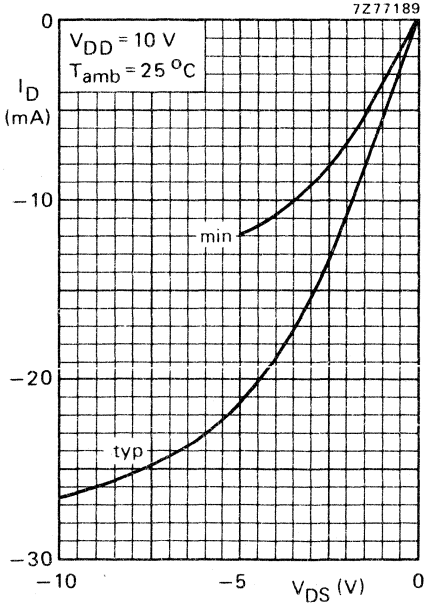
parameter	V_{DD} V	symbol	T_{amb} (°C)						unit	conditions
			−40		+25		+85			
			min	max	min	max	min	max		
Output (sink) current LOW	5	I_{OL}	0,52	–	0,44	–	0,36	–	mA	V_O = 0,4 V; V_I = 0 or 5 V
	10		1,3	–	1,1	–	0,9	–	mA	V_O = 0,5 V; V_I = 0 or 10 V
	15		3,6	–	3,0	–	2,4	–	mA	V_O = 1,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	0,52	–	0,44	–	0,36	–	mA	V_O = 4,6 V; V_I = 0 or 5 V
	10		1,3	–	1,1	–	0,9	–	mA	V_O = 9,5 V; V_I = 0 or 10 V
	15		3,6	–	3,0	–	2,4	–	mA	V_O = 13,5 V; V_I = 0 or 15 V
Output (source) current HIGH	5	$-I_{OH}$	1,7	–	1,4	–	1,1	–	mA	V_O = 2,5 V; V_I = 0 or 5 V
Input leakage current	15	$\pm I_{IN}$	–	0,3	–	0,3	–	1,0	μA	V_I = 0 or 15 V
3-state output leakage current; HIGH	15	I_{OZH}	–	1,6	–	1,6	–	12,0	μA	output returned to V_{DD}
3-state output leakage current; LOW	15	$-I_{OZL}$	–	1,6	–	1,6	–	12,0	μA	output returned to V_{SS}



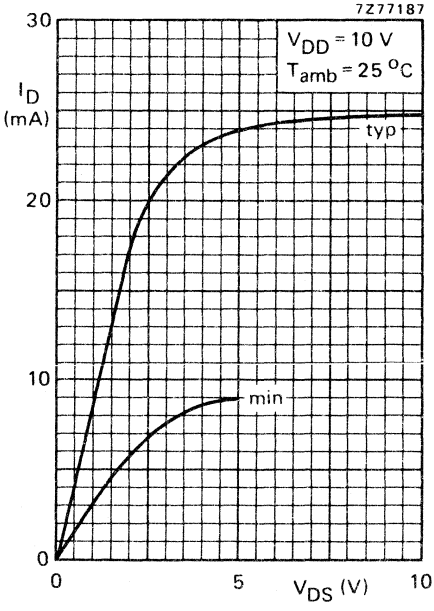
P-channel drain characteristics (source)



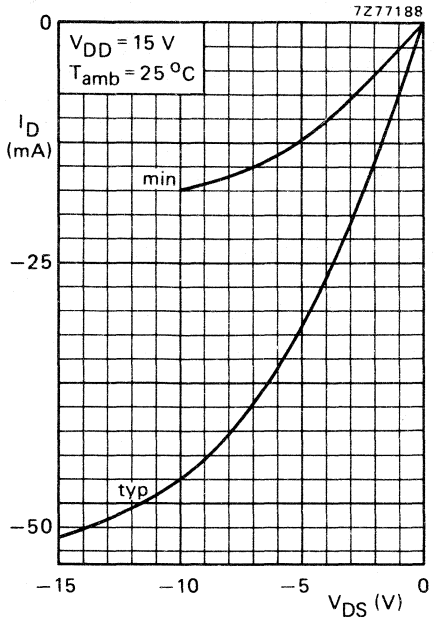
N-channel drain characteristics (sink)



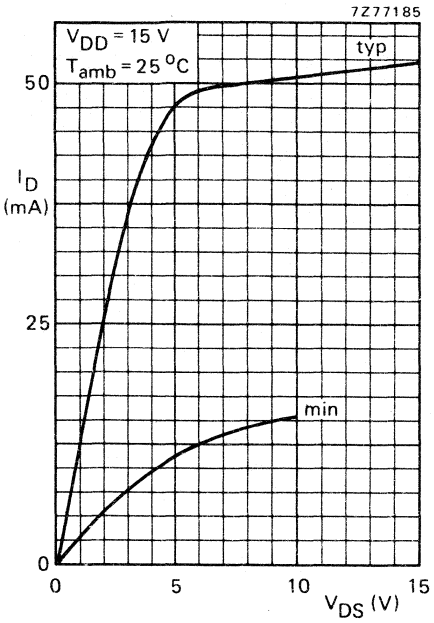
P-channel drain characteristics (source)



N-channel drain characteristics (sink)



P-channel drain characteristics (source)



N-channel drain characteristics (sink)

Note

Temperature coefficient: −0,4%/°C.

A.C. CHARACTERISTICS

Clock input rise and fall times (t_r, t_f)

The upper limits on t_r and t_f vary widely from device to device and with supply voltage. Unless otherwise specified in the individual data sheets it is recommended that input rise and fall times be less than 15 μs for V_{DD} = 5 V; 4 μs for V_{DD} = 10 V; 1 μs for V_{DD} = 15 V.

Output transition times (t_{TLH}, t_{THL})

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times $\leqslant$ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Output transition times							
HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L

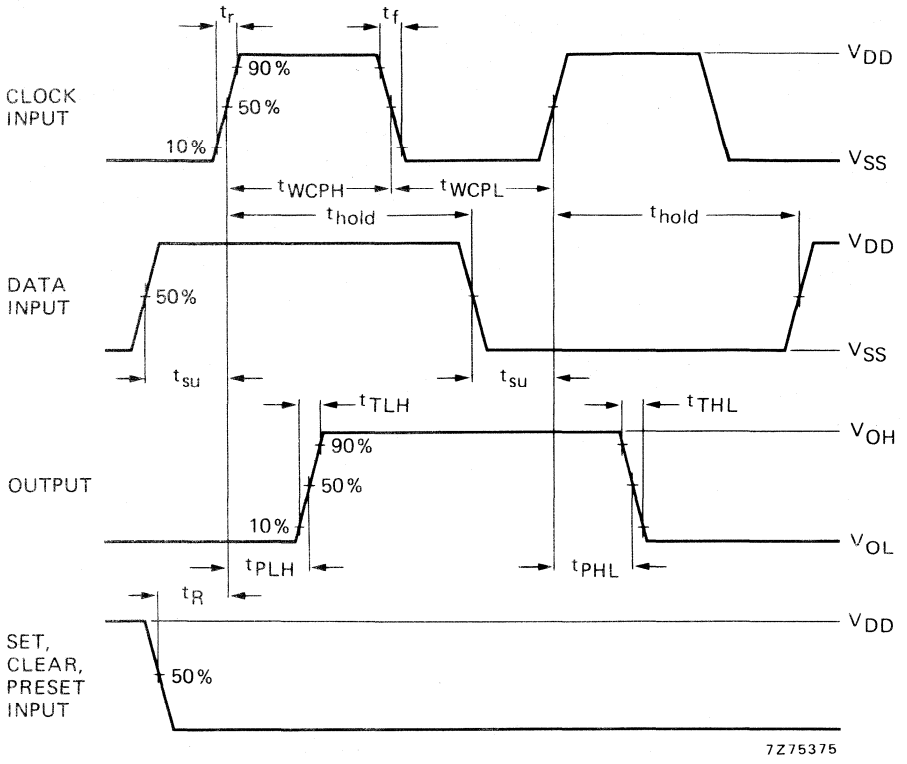
Temperature coefficient (typical values)

Propagation delays	+0,35%/°C
Output transition times	+0,35%/°C

Input capacitance

Maximum input capacitance C_I = 7,5 pF.

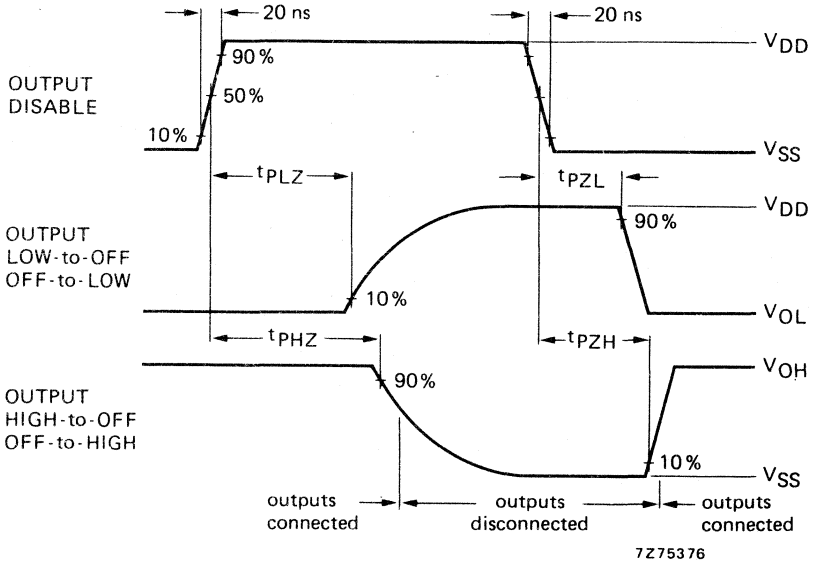
Set-up times, hold times, recovery times and propagation delays for sequential logic circuits.



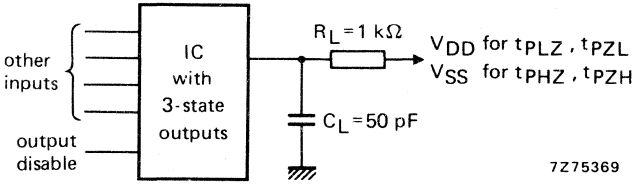
Note

In the waveforms above the active transition of the clock input is going from LOW to HIGH and the active level of the forcing signals (SET, CLEAR and PRESET) is HIGH.
The actual direction of the active transition of the clock input and the actual active levels of the forcing signals are specified in the individual device data sheet.

Propagation delays of 3-state outputs.



Test circuit of 3-state output ICs.



DEFINITION OF SYMBOLS AND TERMS USED IN DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device.

I_{IN} Input current; the current flowing into a device at specified input voltage and V_{DD}.

I_{OH} Output current HIGH; the drive current flowing out of the device at specified HIGH output voltage and V_{DD}.

I_{OL} Output current LOW; the drive current flowing into a device at specified LOW output voltage and V_{DD}.

I_{DD} Quiescent power supply current; the current flowing into the V_{DD} lead at specified input and V_{DD} conditions.

I_{OZ} Output OFF current; the leakage current flowing into or out of the output of a 3-state device in the OFF state when the output is connected to V_{DD} or V_{SS}.

I_{IL} Input current LOW; the current flowing into a device at a specified LOW level input voltage and a specified V_{DD}.

I_{IH} Input current HIGH; the current flowing into a device at a specified HIGH level input voltage and a specified V_{DD}.

I_{DDL} Quiescent power supply current LOW; the current flowing into the V_{DD} lead with a specified LOW level input voltage on all inputs and specified V_{DD} conditions.

I_{DDH} Quiescent power supply current HIGH; the current flowing into the V_{DD} lead with a specified HIGH level input voltage on all inputs and specified V_{DD} conditions.

I_Z OFF state leakage current; the leakage current flowing into the output of a 3-state device in the OFF state at a specified output voltage and V_{DD}.

Voltages

All voltages are referenced to V_{SS}, which is the most negative potential applied to the device.

V_{DD} Supply voltage; the most positive potential on the device.

V_{SS} Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{EE} Supply voltage; one of two (V_{SS} and V_{EE}) negative power supplies. For a device with dual negative power supply, the most negative power supply as a reference level for other voltages.

V_{IH} Input voltage HIGH; the range of input voltages that represents a logic HIGH level in the system.

V_{IL} Input voltage LOW; the range of input voltages that represents a logic LOW level in the system.

V_{OH} Output voltage HIGH; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.

V_{OL} Output voltage LOW; the range of voltages at an output terminal with specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.

Analogue terms

R_{ON} ON resistance; the effective ON state resistance of an analogue transmission gate, at specified input voltage, output load and V_{DD}.

ΔR_{ON} ΔON resistance; the difference in effective ON resistance between any two transmission gates of an analogue device at specified input voltage, output load and V_{DD}.

A.C. switching parameters

f_i Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device truth table. For sequential logic devices the clock frequency using alternate HIGH and LOW for data input or using the toggle mode, whichever is applicable.

f_o Output frequency; each output.

f_{max} Clock frequency; clock input waveform should have a 50% duty cycle and be such as to cause the outputs to be switching from 10% V_{DD} to 90% V_{DD} in accordance with the device truth table.

t_r, t_f Clock input rise and fall times; 10% to 90% value.

t_{PLH} Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation delay time; the time between the specified reference points, normally 50% points on the input and output waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_{TLH} Transition time, LOW-to-HIGH; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from LOW to HIGH.

t_{THL} Transition time, HIGH-to-LOW; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from HIGH to LOW.

t_W Pulse width; the time between 50% amplitude points on the leading and trailing edges of pulse.

t_{hold} Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_{su} Set-up time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their recognition. A negative set-up time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} 3-state output disable time, HIGH to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 V_{OH} drop on the output voltage waveform of a 3-state device, with the output changing from the output HIGH level (V_{OH}) to a high impedance OFF-state.

t_{PLZ} 3-state output disable time, LOW to Z; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing a 0,1 ($V_{DD}-V_{OL}$) rise on the output voltage waveform of a 3-state device, with the output changing from the output LOW level (V_{OL}) to a high impedance OFF-state.

t_{PZH} 3-state output enable time, Z to HIGH; the time between the specified reference points, normally 50% point on the output enable input voltage waveform and a point representing 0,1 V_{OH} voltage rise on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output HIGH level (V_{OH}).

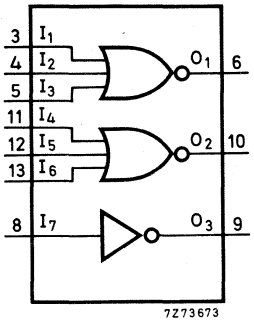
t_{PZL} 3-state output enable time, Z to LOW; the time between the specified reference points, normally the 50% point on the output enable input voltage waveform and a point representing 0,1 ($V_{DD}-V_{OL}$) voltage drop on the output voltage waveform of a 3-state device, with the output changing from a high impedance OFF-state to the output LOW level (V_{OL}).

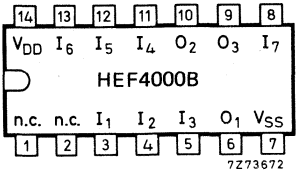
t_R Recovery time; the time between the end of an overriding asynchronous input, typically a clear or reset input, and the earliest permissible beginning of a synchronous control input, typically a clock input, normally measured at 50% points on both input voltage waveforms.

DEVICE DATA

DUAL 3-INPUT NOR GATE AND INVERTER

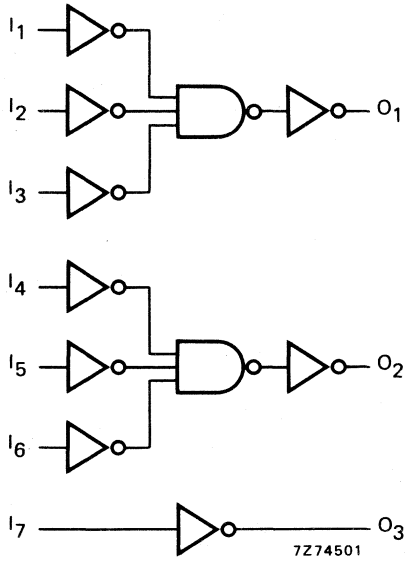
The HEF4000B provides the positive dual 3-input NOR function. An inverting function is also accomplished. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4000BP : 14-lead DIL; plastic (SOT-27).
HEF4000BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA see Family Specifications

I_{DD} LIMITS category GATES see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Inverter input voltage HIGH	5	V_{IH}	4,0	–	4,0	–	4,0	–	V
	10		8,0	–	8,0	–	8,0	–	V
	15		12,5	–	12,5	–	12,5	–	V
Inverter input voltage LOW	5	V_{IL}	–	1,0	–	1,0	–	1,0	V
	10		–	2,0	–	2,0	–	2,0	V
	15		–	2,5	–	2,5	–	2,5	V

A.C. CHARACTERISTICS

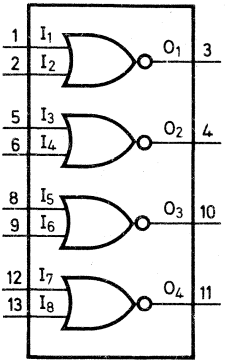
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays I_1 to I_6 → O_1, O_2	5	t_{PHL}; t_{PLH}	70	140	ns	43 ns + (0,55 ns/pF) C_L
	10		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
I_7 → O_3	5	t_{PHL}; t_{PLH}	45	90	ns	18 ns + (0,55 ns/pF) C_L
	10		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$7700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$28\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT NOR GATE

The HEF4001B provides the positive quadruple 2-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



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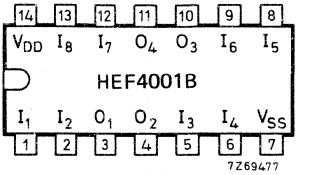

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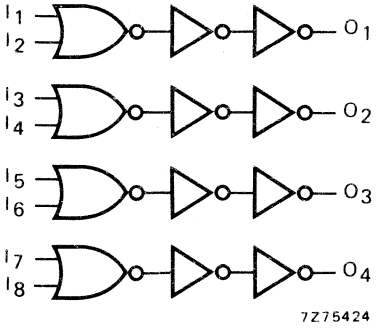
HEF4001BP: 14-lead DIL; plastic (SOT-27).
HEF4001BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



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FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

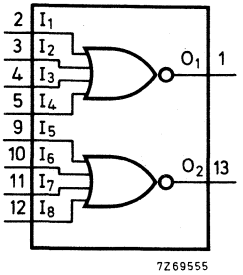
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

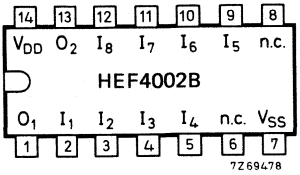
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		50	100	ns	23 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	14 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

DUAL 4-INPUT NOR GATE

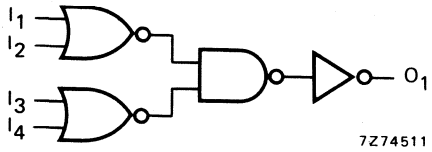
The HEF4002B provides the positive dual 4-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4002BP : 14-lead DIL; plastic (SOT-27).
HEF4002BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

$V_{SS} = 0$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF; input transition times $\leqslant 20$ ns

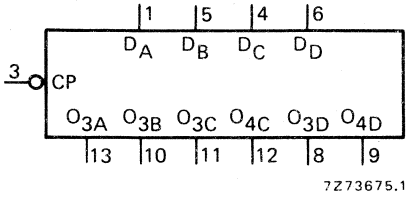
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	t_{PHL}; t_{PLH}	60	120	ns	33 ns + (0,55 ns/pF) C_L
	10		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L

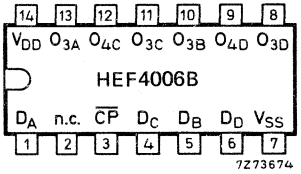
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1050\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

18-STAGE STATIC SHIFT REGISTER

The HEF4006B is an 18-stage shift register arranged as two 4-stage and two 5-stage shift registers with a common clock input ($\overline{CP}$). The two 4-stage shift registers each have a data input (D_A, D_B) and a data output (O_{3A}, O_{3B}); the two 5-stage shift registers each have a data input (D_C, D_D) and data outputs from the fourth and fifth stages (O_{3C}, O_{4C}, O_{3D}, O_{4D}).

The registers can be operated in parallel or interconnected to form a single shift register of up to 18 bits. Data are shifted into the first register position of each register from the data inputs (D_A to D_D) and all the data in each register are shifted one position to the right on the HIGH to LOW transition of $\overline{CP}$.





HEF4006BP: 14-lead DIL; plastic (SOT-27).
HEF4006BD: 14-lead DIL; ceramic (SOT-73).

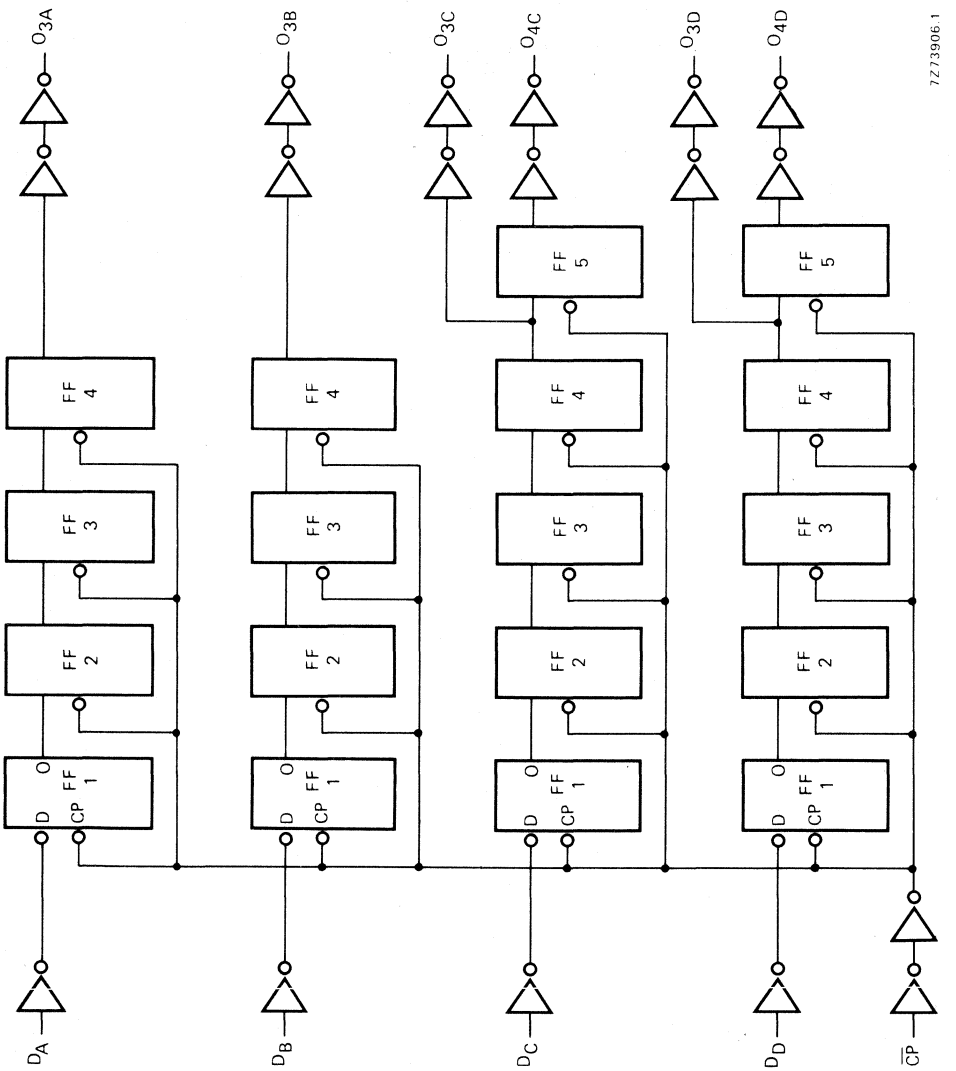
PINNING

D_A to D_D	data inputs
$\overline{CP}$	clock input (HIGH to LOW; edge-triggered)
O_{3A} to O_{3D}; O_{4C}; O_{4D}	data outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM

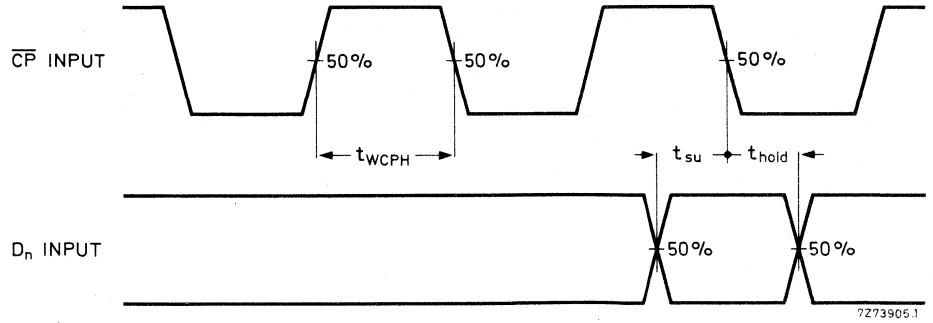


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{CP} \rightarrow O_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
Minimum clock pulse width; HIGH	5		60	30		ns	see also waveforms below
	10	t_{WCPH}	40	20		ns	
	15		30	15		ns	
Set-up time $D_n \rightarrow \overline{CP}$	5		20	10		ns	
	10	t_{su}	10	5		ns	
	15		5	0		ns	
Hold time $D_n \rightarrow \overline{CP}$	5		5	−5		ns	
	10	t_{hold}	5	0		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5		9	18		MHz	
	10	f_{max}	15	30		MHz	
	15		18	36		MHz	

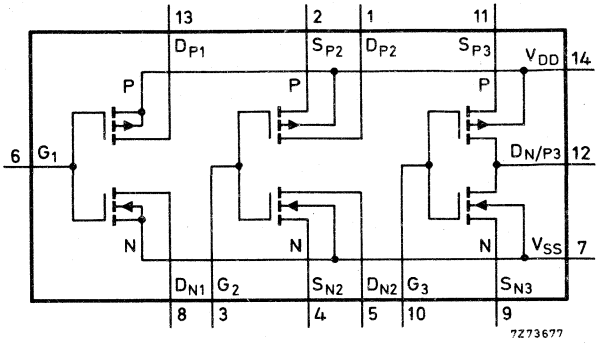
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	3200 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	11 600 f_i + Σ($f_o C_L$) x V_{DD}^2	

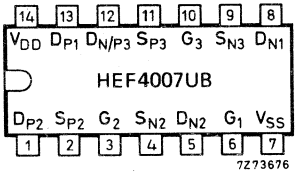


Waveforms showing minimum clock pulse width, and set-up and hold times for D_n to $\overline{CP}$.
Set-up and hold times are shown as positive values but may be specified as negative values.

DUAL COMPLEMENTARY PAIR AND INVERTER

The HEF4007UB is a dual complementary pair and an inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors.





HEF4007UBP: 14-lead DIL; plastic (SOT-27).
HEF4007UBD: 14-lead DIL; ceramic (SOT-73).

PINNING

S_{P2}, S_{P3}	source connections to 2nd and 3rd p-channel transistors
D_{P1}, D_{P2}	drain connections from the 1st and 2nd p-channel transistors
D_{N1}, D_{N2}	drain connections from the 1st and 2nd n-channel transistors
S_{N2}, S_{N3}	source connections to the 2nd and 3rd n-channel transistors
$D_{N/P3}$	common connection to the 3rd p-channel and n-channel transistor drains
G_1 to G_3	gate connections to n-channel and p-channel of the three transistor pairs

FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Input voltage HIGH	5	V_{IH}	4,0	–	4,0	–	4,0	–	V
	10		8,0	–	8,0	–	8,0	–	V
	15		12,5	–	12,5	–	12,5	–	V
Input voltage LOW	5	V_{IL}	–	1,0	–	1,0	–	1,0	V
	10		–	2,0	–	2,0	–	2,0	V
	15		–	2,5	–	2,5	–	2,5	V

A.C. CHARACTERISTICS

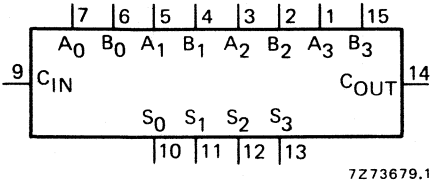
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

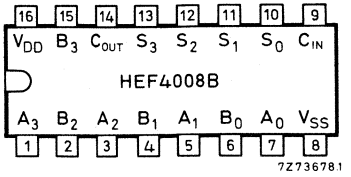
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $G_n \rightarrow D_N$; D_P HIGH to LOW	5	t_{PHL}	40	80	ns	13 ns + (0,55 ns/pF) C_L
	10		20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	40	75	ns	13 ns + (0,55 ns/pF) C_L
	10		20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$20\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$50\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

4-BIT BINARY FULL ADDER

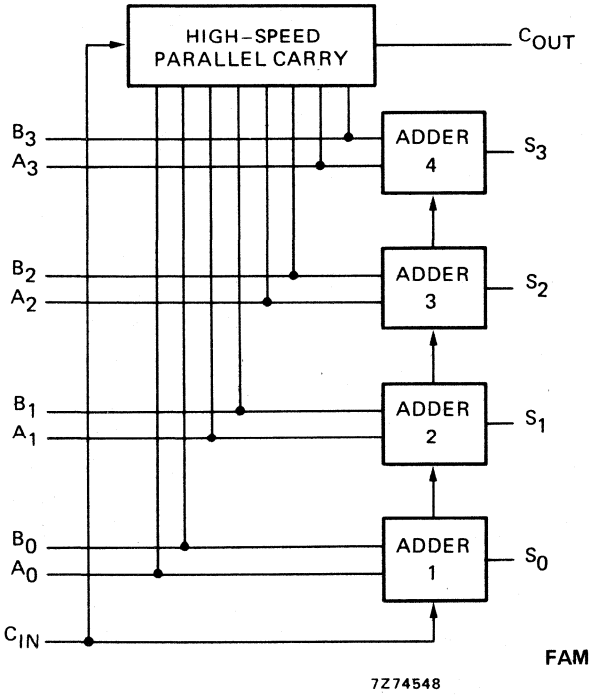
The HEF4008B is a 4-bit binary full adder with two 4-bit data inputs (A_0 to A_3, B_0 to B_3), a carry input (C_{IN}), four sum outputs (S_0 to S_3), and a carry output (C_{OUT}). The IC uses full look-ahead across 4-bits to generate C_{OUT}. This minimizes the necessity for extensive look-ahead and carry-cascading circuits.





HEF4008BP: 16-lead DIL; plastic (SOT-38Z).
HEF4008BD: 16-lead DIL; ceramic (SOT-74).

BLOCK DIAGRAM



TRUTH TABLE (one adder)

C_{IN}	A	B	C_{OUT}	S
L	L	L	L	L
L	L	H	L	H
L	H	L	L	H
L	H	H	H	L
H	L	L	L	H
H	L	H	H	L
H	H	L	H	L
H	H	H	H	H

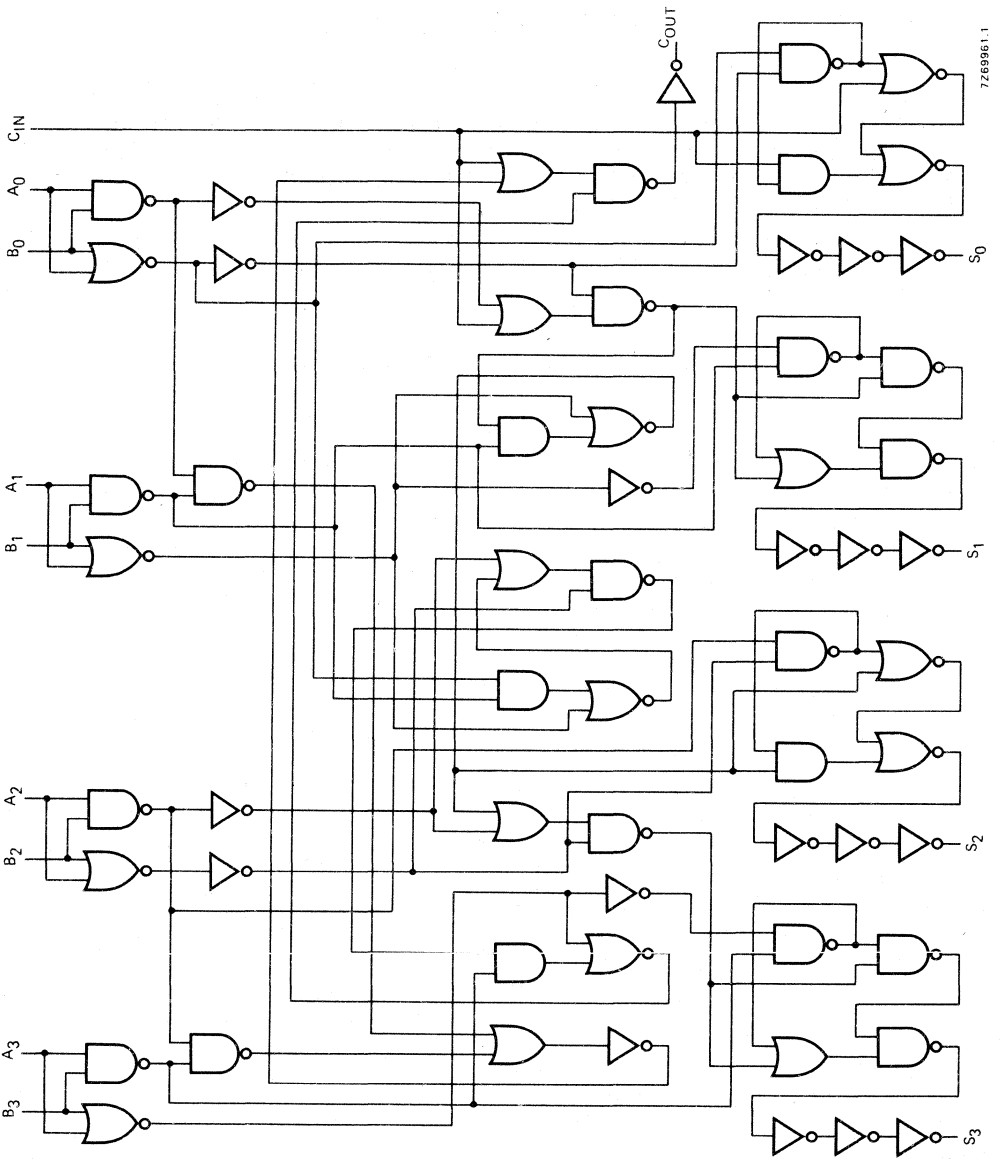
PINNING

A_0 to A_3	data inputs
B_0 to B_3	data inputs
S_0 to S_3	sum outputs
C_{IN}	carry input
C_{OUT}	carry output

FAMILY DATA } see Family Specifications

I_{DD} LIMITS category MSI }

LOGIC DIAGRAM



A.C. CHARACTERISTICS

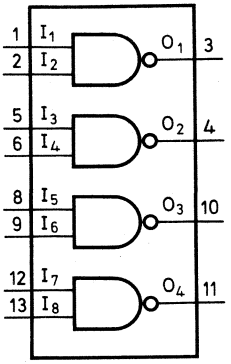
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

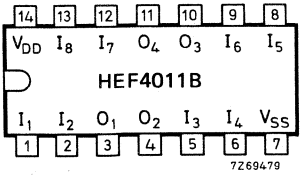
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
A_n, B_n → S_n	5			125	245 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			110	225 ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	75 ns	27 ns + (0,16 ns/pF) C_L
A_n, B_n → C_{OUT}	5			140	285 ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	125 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			115	225 ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
C_{IN} → S_n	5			100	200 ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
	5			95	190 ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
C_{IN} → C_{OUT}	5			70	140 ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	60 ns	19 ns + (0,23 ns/pF) C_L
	15			20	45 ns	12 ns + (0,16 ns/pF) C_L
	5			60	120 ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	55 ns	14 ns + (0,23 ns/pF) C_L
	15			20	40 ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	9900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	32 300 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT NAND GATE

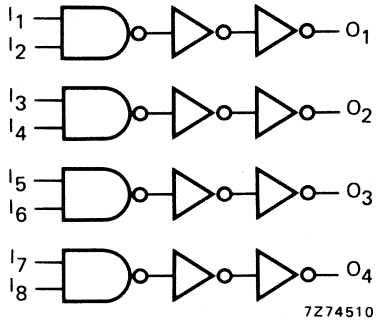
The HEF4011B provides the positive quadruple 2-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4011BP : 14-lead DIL; plastic (SOT-27).
HEF4011BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

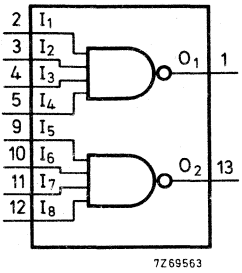
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

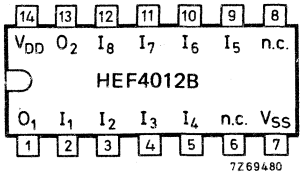
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	t_{PHL}; t_{PLH}	55	110	ns	28 ns + (0,55 ns/pF) C_L
	10		25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$20\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 4-INPUT NAND GATE

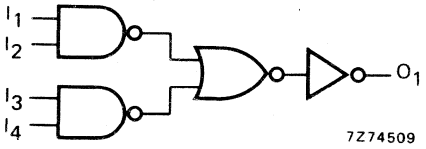
The HEF4012B provides the positive dual 4-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4012BP : 14-lead DIL; plastic (SOT-27).
HEF4012BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

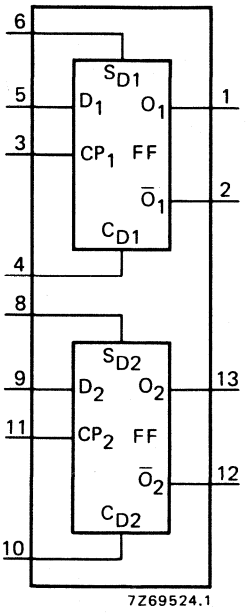
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

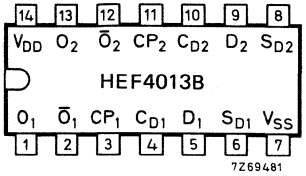
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		70	135	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
	5		70	140	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$12\,900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL D-TYPE FLIP-FLOP

The HEF4013B is a dual D-type flip-flop which is edge-triggered and features independent set direct, clear direct, and clock inputs. Data is accepted when CP is LOW and transferred to the output on the positive-going edge of the clock.
The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the D or CP inputs. The outputs are buffered for best system performance.





HEF4013BP: 14-lead DIL; plastic (SOT–27).
HEF4013BD: 14-lead DIL; ceramic (SOT–73).

TRUTH TABLES

inputs				outputs	
S_D	C_D	CP	D	O	$\overline{O}$
H	L	X	X	H	L
L	H	X	X	L	H
H	H	X	X	H	H

inputs				outputs	
S_D	C_D	CP	D	O_{n+1}	$\overline{O}_{n+1}$
L	L	∫	L	L	H
L	L	∫	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

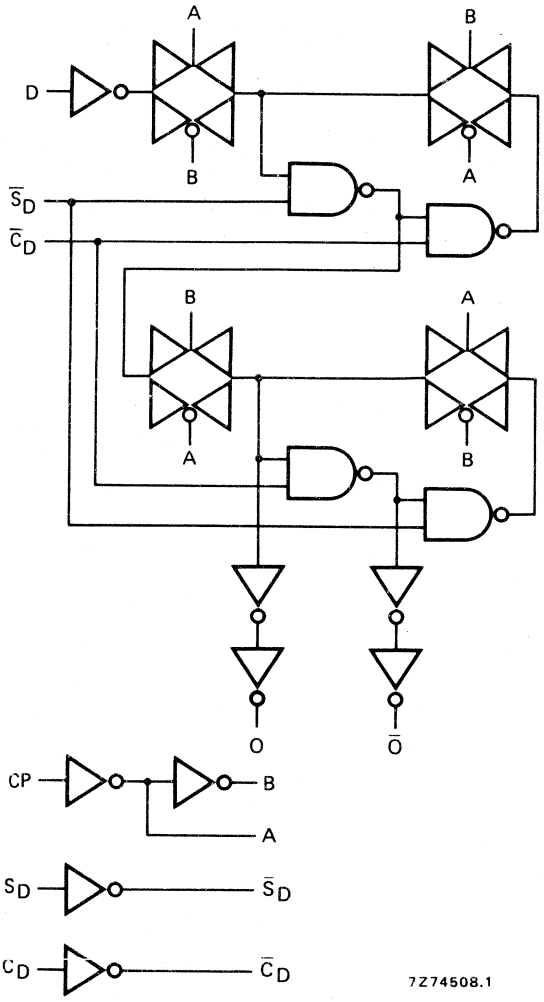
PINNING

D data inputs
CP clock input (L to H edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\overline{O}$ complement output

FAMILY DATA

I_{DD} LIMITS category FLIP-FLOPS } see Family Specifications

LOGIC DIAGRAM (one flip-flop)



A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

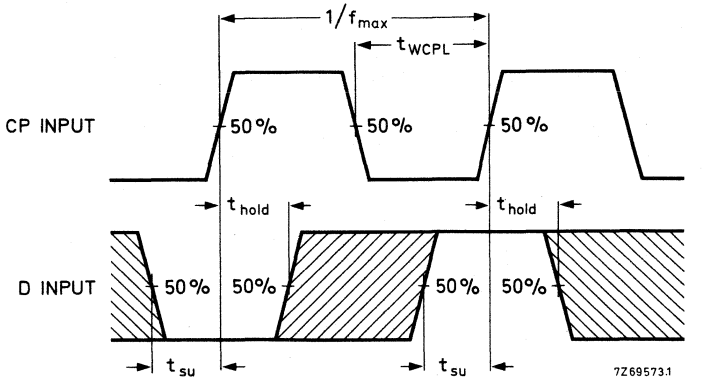
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O, $\overline{O}$	5			105	205	ns	78 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF)C_L
	15			25	55	ns	17 ns + (0,16 ns/pF)C_L
	5			100	205	ns	73 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF)C_L
	15			30	60	ns	22 ns + (0,16 ns/pF)C_L
S_D → $\overline{O}$	5			70	135	ns	43 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		25	55	ns	14 ns + (0,23 ns/pF)C_L
	15			20	40	ns	12 ns + (0,16 ns/pF)C_L
S_D → O	5			135	265	ns	108 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF)C_L
	15			35	70	ns	27 ns + (0,16 ns/pF)C_L
C_D → O	5			90	180	ns	63 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		35	75	ns	24 ns + (0,23 ns/pF)C_L
	15			25	55	ns	17 ns + (0,16 ns/pF)C_L
C_D → $\overline{O}$	5			115	225	ns	88 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		50	95	ns	39 ns + (0,23 ns/pF)C_L
	15			35	75	ns	27 ns + (0,16 ns/pF)C_L
Set-up time	5		60	30		ns	
D → CP	10	t_{su}	30	10		ns	
	15		30	10		ns	
Hold time	5		20	−10		ns	
D → CP	10	t_{hold}	20	0		ns	
	15		20	0		ns	
Minimum clock	5		85	45		ns	
pulse width; LOW	10	t_{WCPL}	40	20		ns	
	15		30	15		ns	
Minimum S_D pulse	5		65	35		ns	see also waveforms on page 5
width; HIGH	10	t_{WSDH}	35	20		ns	
	15		30	15		ns	
Minimum C_D pulse	5		90	45		ns	
width; HIGH	10	t_{WCDH}	40	20		ns	
	15		35	20		ns	
Recovery time	5		20	10		ns	
for S_D	10	t_{RSD}	15	5		ns	
	15		15	5		ns	
Recovery time	5		0	−10		ns	
for C_D	10	t_{RCD}	5	−5		ns	
	15		5	−5		ns	

A.C. CHARACTERISTICS

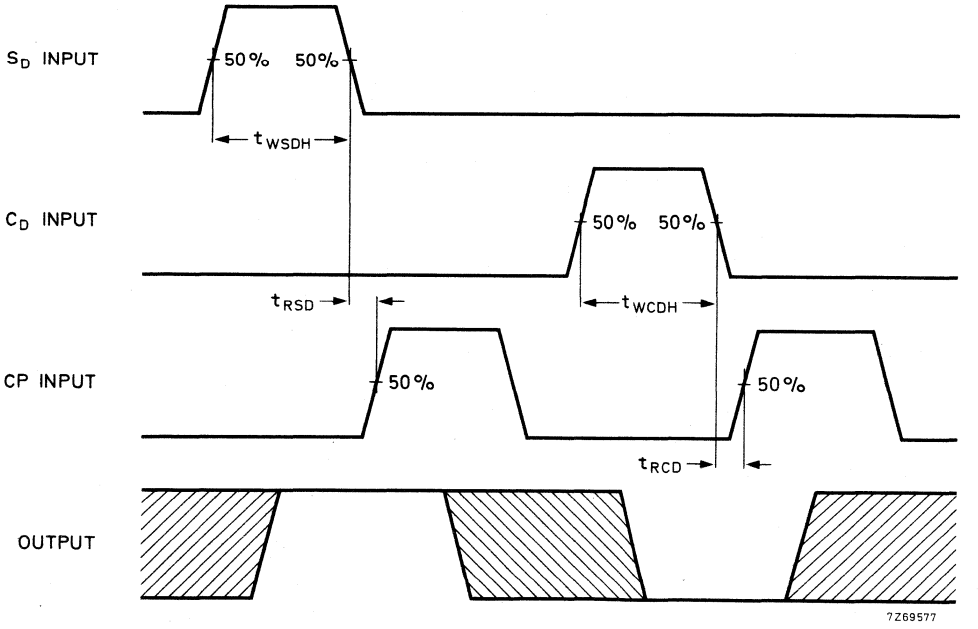
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Maximum clock pulse frequency	5	f_{max}	6	12	MHz	
	10		12	25	MHz	
	15		18	36	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1050\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = total load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,350\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

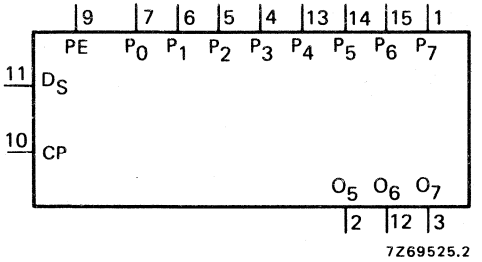


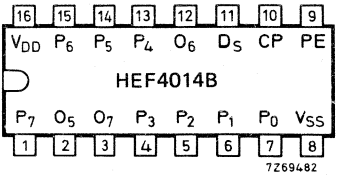
Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.

8-BIT SHIFT REGISTER

The HEF4014B is a fully synchronous edge-triggered 8-bit shift register with eight synchronous parallel inputs (P_0 to P_7), a synchronous serial data input (D_S), a synchronous parallel enable input (PE), a LOW to HIGH edge-triggered clock input (CP) and buffered parallel outputs from the last three stages (O_5 to O_7).

Operation is synchronous and the device is edge-triggered on the LOW to HIGH transition of CP. When PE is HIGH, data is loaded into the register from P_0 to P_7 on the LOW to HIGH transition of CP. When PE is LOW, data is shifted to the first register position from D_S, and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP.





HEF4014BP: 16-lead DIL; plastic (SOT-38Z).
HEF4014BD: 16-lead DIL; ceramic (SOT-74).

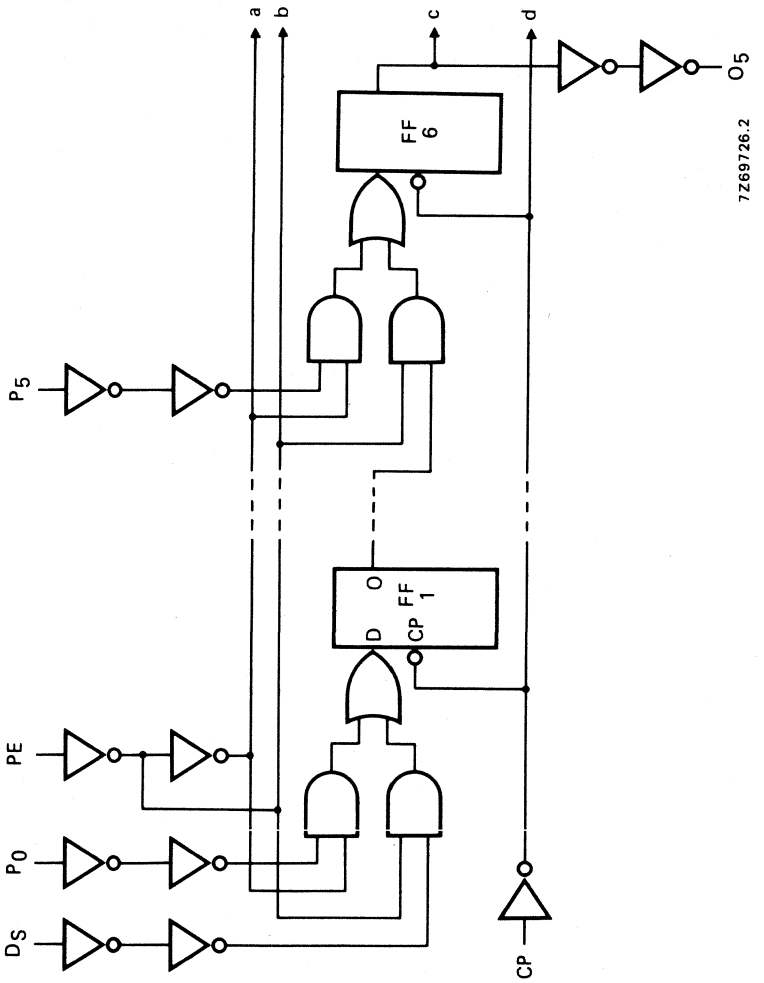
PINNING

PE	parallel enable input
P_0 to P_7	parallel data inputs
D_S	serial data input
CP	clock input (LOW to HIGH edge-triggered)
O_5 to O_7	buffered parallel outputs from the last three stages

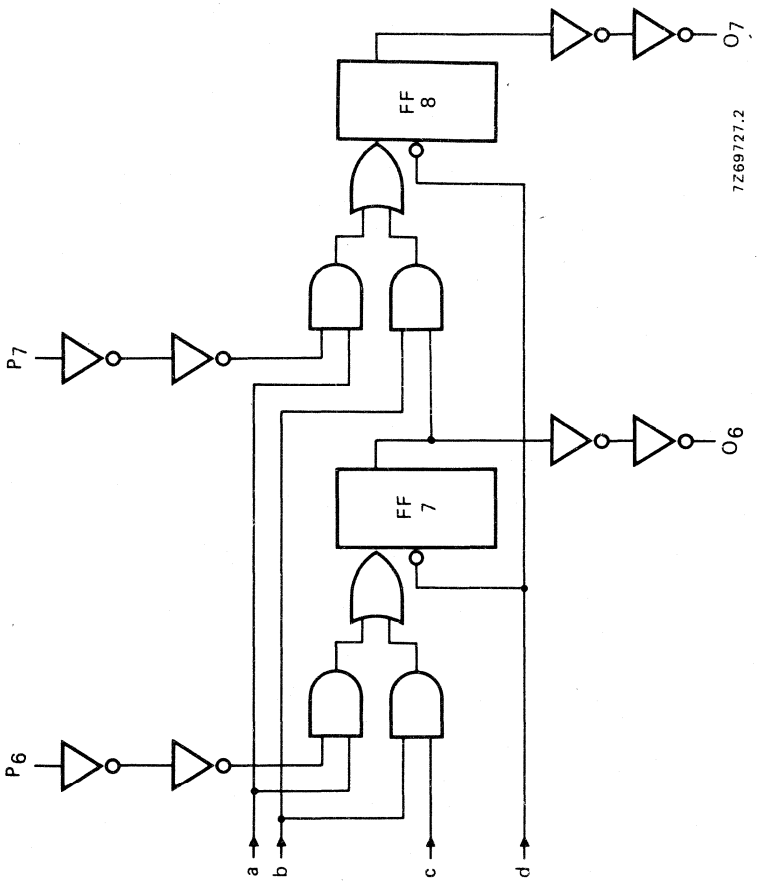
FAMILY DATA

I_{DD} LIMITS category MSI — see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



TRUTH TABLES

Serial operation

n	inputs			outputs		
	CP	D_S	PE	O_5	O_6	O_7
1	⎍	D_1	L	X	X	X
2	⎍	D_2	L	X	X	X
3	⎍	D_3	L	X	X	X
6	⎍	X	L	D_1	X	X
7	⎍	X	L	D_2	D_1	X
8	⎍	X	L	D_3	D_2	D_1
	⎎	X	X	no change		

Parallel operation

n	inputs			outputs		
	CP	D_S	PE	O_5	O_6	O_7
1	⎍	X	H	P_5	P_6	P_7
	⎎	X	X	no change		

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going transition
⎎ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

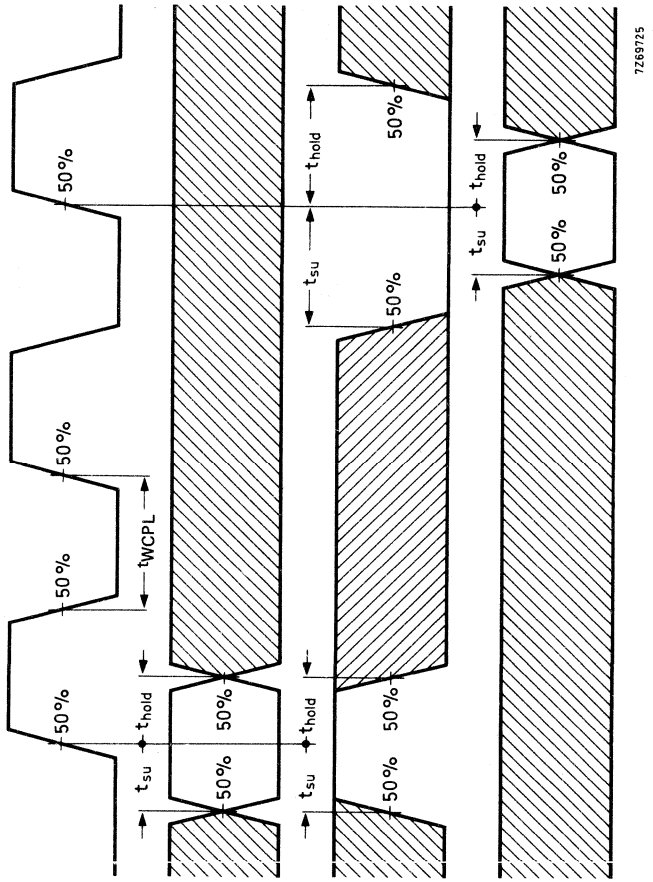
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP → O_n	5			145	290 ns	118 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF)C_L
	15			45	90 ns	37 ns + (0,16 ns/pF)C_L
	5			110	225 ns	83 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		50	100 ns	39 ns + (0,23 ns/pF)C_L
	15			40	75 ns	32 ns + (0,16 ns/pF)C_L
Set-up times	5		180	90	ns	
PE → CP	10	t_{su}	70	35	ns	
	15		50	25	ns	
	5		110	55	ns	
D_S → CP	10	t_{su}	40	20	ns	
	15		30	15	ns	
	5		160	80	ns	
P_n → CP	10	t_{su}	60	30	ns	
	15		40	20	ns	see also waveforms on page 6
Hold times	5		35	−55	ns	
PE → CP	10	t_{hold}	15	−20	ns	
	15		10	−15	ns	
	5		10	−45	ns	
D_S → CP	10	t_{hold}	5	−15	ns	
	15		0	−15	ns	
	5		10	−70	ns	
P_n → CP	10	t_{hold}	5	−25	ns	
	15		5	−15	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55		ns	see also waveforms on page 6
	10		45	20		ns	
	15		30	15		ns	
Maximum clock pulse frequency	5	f_{max}	5	9		MHz	
	10		11	22		MHz	
	15		16	32		MHz	

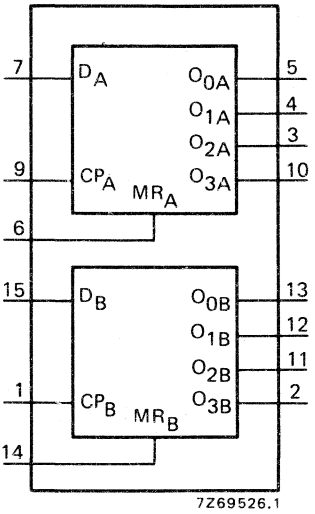
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5250\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\ 700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

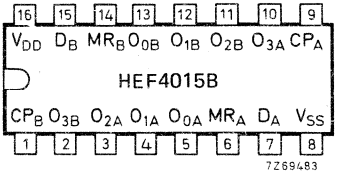


Waveforms showing minimum clock pulse width, and set-up and hold times for PE to CP, D_S to CP, and P to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

DUAL 4-BIT STATIC SHIFT REGISTER

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (O_0 to O_3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces O_0 to O_3 to LOW, independent of CP and D.





HEF4015BP: 16-lead DIL; plastic (SOT-38Z).
HEF4015BD: 16-lead DIL; ceramic (SOT-74).

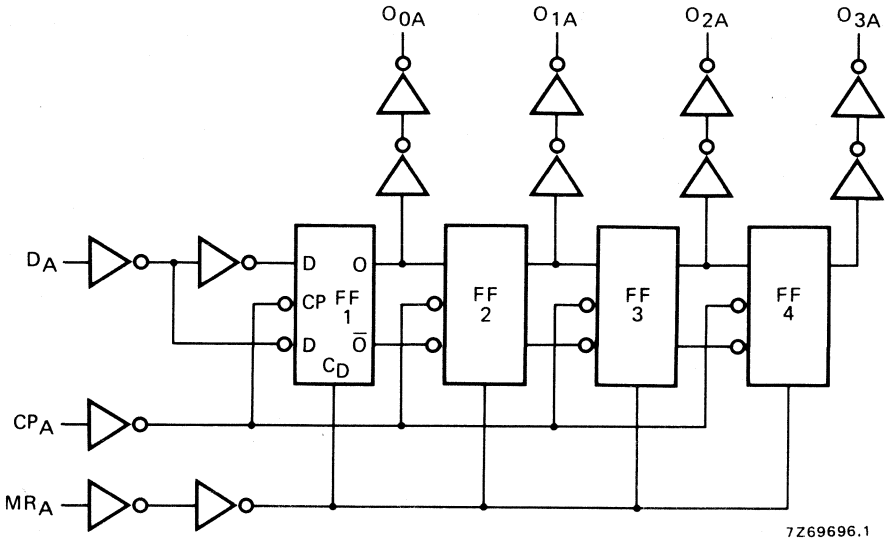
PINNING

D_A, D_B	serial data input
MR_A, MR_B	master reset input (active HIGH)
CP_A, CP_B	clock input (LOW-to-HIGH edge-triggered)
O_{0A}, O_{1A}, O_{2A}, O_{3A}	parallel outputs
O_{0B}, O_{1B}, O_{2B}, O_{3B}	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM (one register)



TRUTH TABLE

	inputs			outputs			
n	CP	D	MR	O_0	O_1	O_2	O_3
1	∫	D_1	L	D_1	X	X	X
2	∫	D_2	L	D_2	D_1	X	X
3	∫	D_3	L	D_3	D_2	D_1	X
4	⌝	D_4	L	D_4	D_3	D_2	D_1
	∫	X	L	no change			
	X	X	H	L	L	L	L

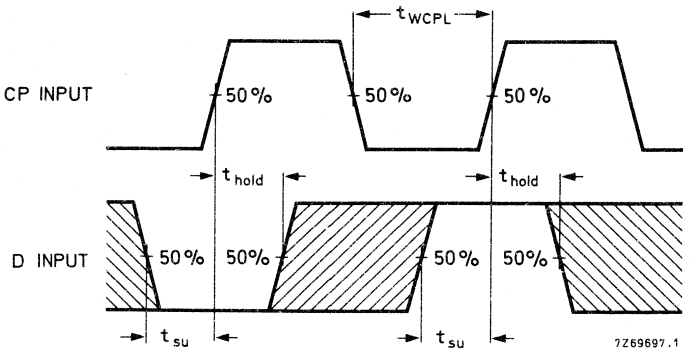
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

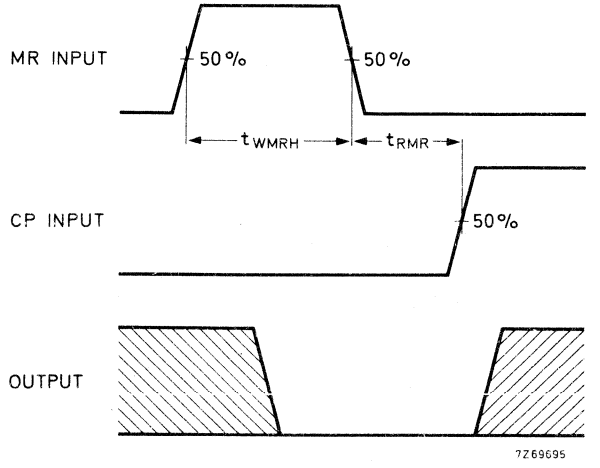
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			145	290	ns	118 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
	5			120	240	ns	93 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF)C_L
	15			40	75	ns	32 ns + (0,16 ns/pF)C_L
MR → O_n	5			185	370	ns	158 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF)C_L
	15			40	85	ns	32 ns + (0,16 ns/pF)C_L
Set-up time	5		110	55		ns	
D → CP	10	t_{su}	30	15		ns	
	15		20	10		ns	
Hold time	5		20	−35		ns	
D → CP	10	t_{hold}	5	−10		ns	
	15		5	−5		ns	
Minimum clock	5		100	50		ns	
pulse width; LOW	10	t_{WCPL}	35	20		ns	
	15		30	15		ns	see waveforms
Minimum MR	5		110	55		ns	on page 4
pulse width; HIGH	10	t_{WMRH}	35	20		ns	
	15		30	15		ns	
Recovery time	5		110	65		ns	
for MR	10	t_{RMR}	40	20		ns	
	15		25	15		ns	
Maximum clock	5		4	9		MHz	
pulse frequency	10	f_{max}	12	23		MHz	
	15		17	34		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1500 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	7800 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	26 100 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	



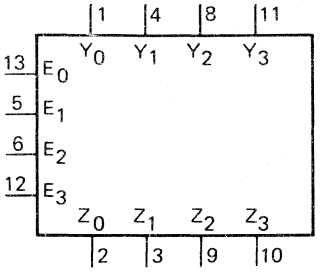
Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

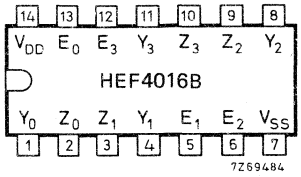


Waveforms showing recovery time for MR and minimum MR pulse width.

QUADRUPLE BILATERAL SWITCHES

The HEF4016B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). A HIGH on E establishes a low impedance bidirectional path between Y and Z (ON condition). A LOW on E disables the switch and establishes a high impedance between Y and Z (OFF condition).



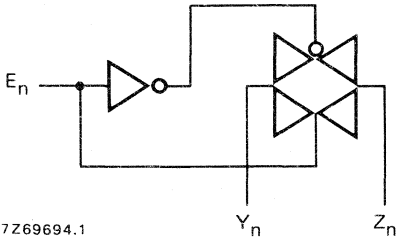


HEF4016BP: 14-lead DIL; plastic (SOT-27).
HEF4016BD: 14-lead DIL; ceramic (SOT-73).

PINNING

E_0 to E_3	enable inputs
Y_0 to Y_3	input/output terminals
Z_0 to Z_3	input/output terminals

LOGIC DIAGRAM (one switch)



FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	8000	–	Ω	E_n at V_{DD}; V_i = V_{SS} to V_{DD}; see Fig. 1
	10		230	690	Ω	
	15		115	350	Ω	
ON resistance	5	R_{ON}	140	425	Ω	E_n at V_{DD}; V_i = V_{SS}; see Fig. 1
	10		65	195	Ω	
	15		50	145	Ω	
ON resistance	5	R_{ON}	170	515	Ω	E_n at V_{DD}; V_i = V_{DD}; see Fig. 1
	10		95	285	Ω	
	15		75	220	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	200	–	Ω	E_n at V_{DD}; V_i = V_{SS} to V_{DD}; see Fig. 1
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, any channel OFF	5	I_{OZ}	–	–	nA	E_n at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$3500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

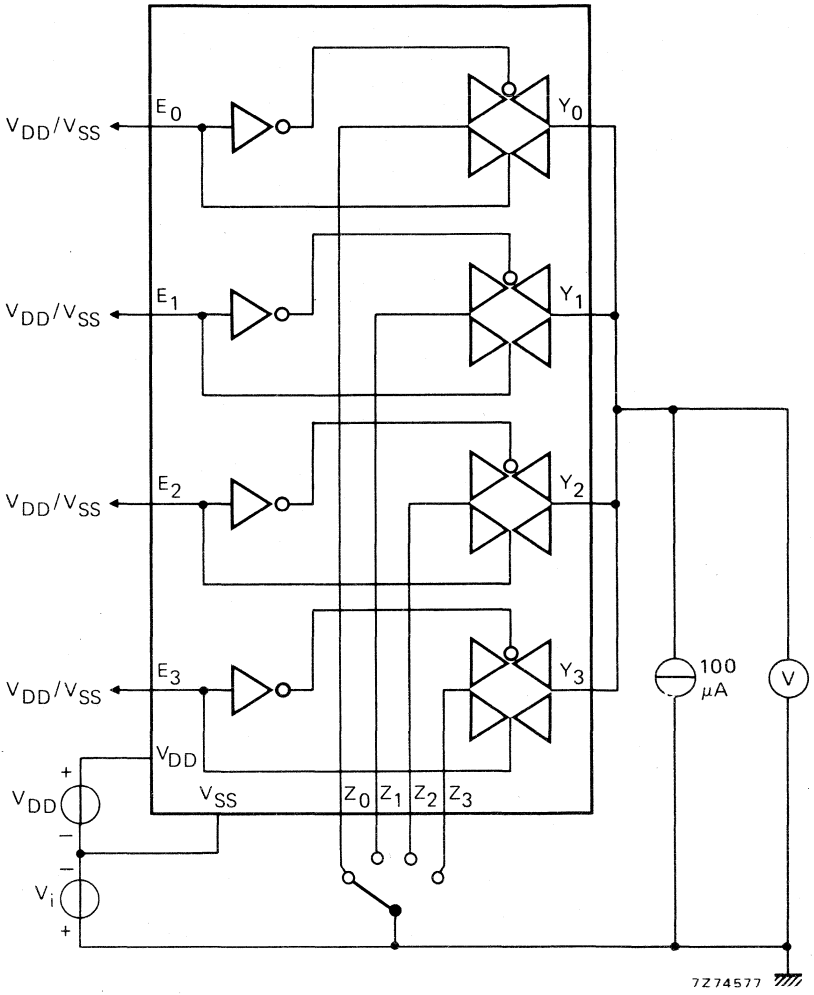


Fig. 1 Test set-up for measuring R_{ON}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		25	50	ns	
HIGH to LOW	10	t_{PHL}	10	20	ns	note 1
	15		5	10	ns	
	5		20	40	ns	
LOW to HIGH	10	t_{PLH}	10	20	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		95	190	ns	
HIGH	10	t_{PHZ}	85	170	ns	note 2
	15		85	170	ns	
	5		50	100	ns	
LOW	10	t_{PLZ}	55	110	ns	note 2
	15		60	120	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		35	70	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		35	70	ns	
LOW	10	t_{PZL}	15	30	ns	note 2
	15		10	20	ns	
Distortion, sine-wave	5		–		%	
response	10		0,08		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n at V_{DD}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} at V_{SS} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
3. R_L = 10 kΩ; C_L = 15 pF; E_n at V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig. 3.
4. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}\ (B)}{V_{is}\ (A)}$ = −50 dB; E_n (A) at V_{SS}; E_n (B) at V_{DD}; see Fig.4.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value);
   see Fig. 2.
6. R_L = 1 kΩ; C_L = 5 pF; E_n at V_{SS}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −50 dB; see Fig.3.
7. R_L = 1 kΩ; C_L = 5 pF; E_n at V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −3 dB; see Fig. 3.

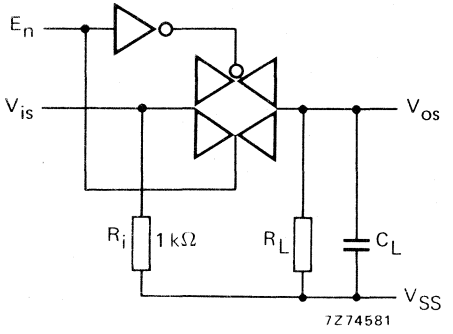


Fig. 2

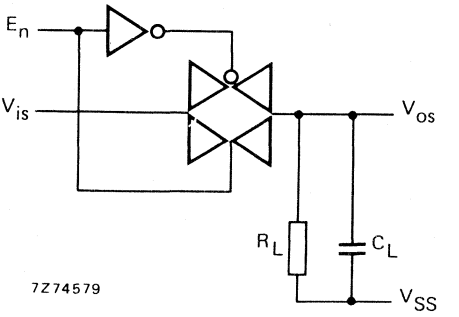
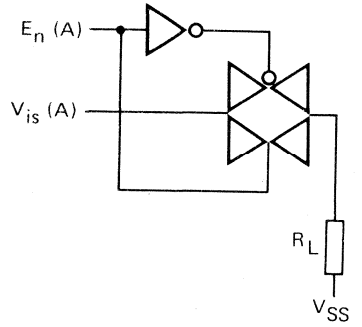
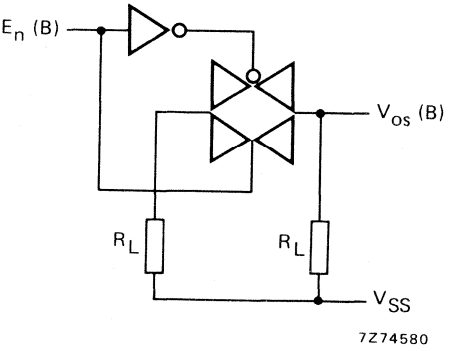


Fig. 3



(a)



(b)

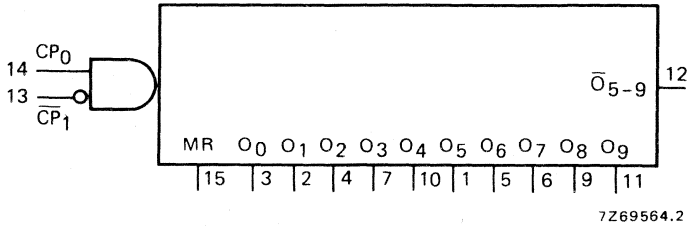
Fig. 4

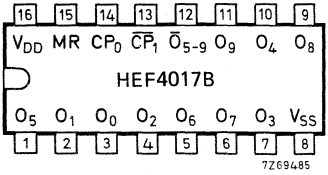
5-STAGE JOHNSON COUNTER

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop ($\overline{O}_{5-9}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also truth table on page 3).
When cascading counters, the $\overline{O}_{5-9}$ output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{5-9}$ = HIGH; O_1 to O_9 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).





HEF4017BP : 16-lead DIL; plastic (SOT-38Z).
HEF4017BD: 16-lead DIL; ceramic (SOT-74).

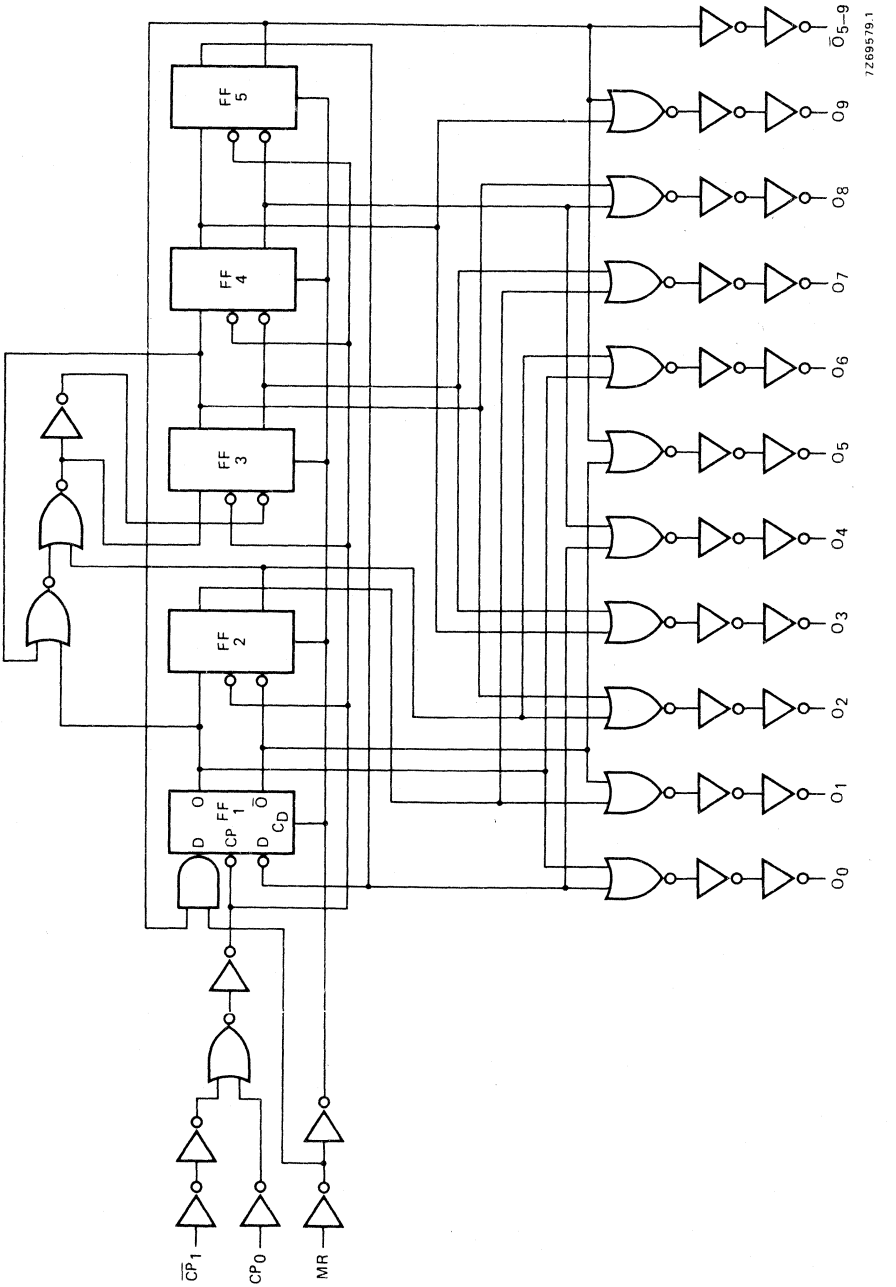
PINNING

CP_0	clock input (LOW to HIGH triggered)
$\overline{CP}_1$	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_9	decoded outputs
$\overline{O}_{5-9}$	carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



LOGIC DIAGRAM

FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{5\text{-}9}$ = H; O_1 to O_9 = L
L	H	↘	Counter advances
L	↗	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	↗	No change
L	↘	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

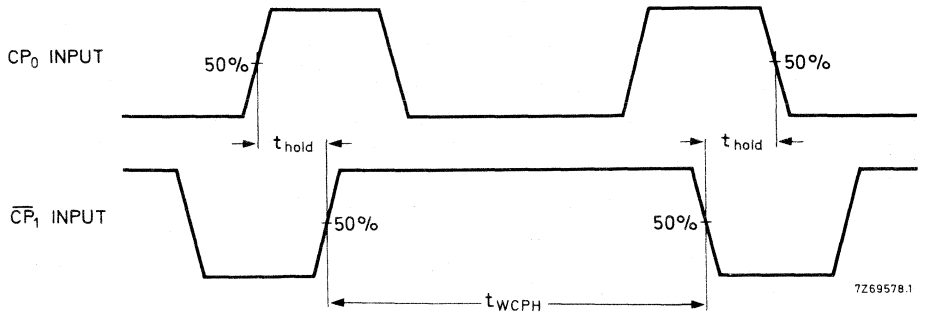
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	195	ns	84 ns + (0,23 ns/pF) C_L
	15			60	125	ns	52 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → $\overline{O}_{5\text{-}9}$	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	185	ns	79 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
MR → $\overline{O}_{5\text{-}9}$	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

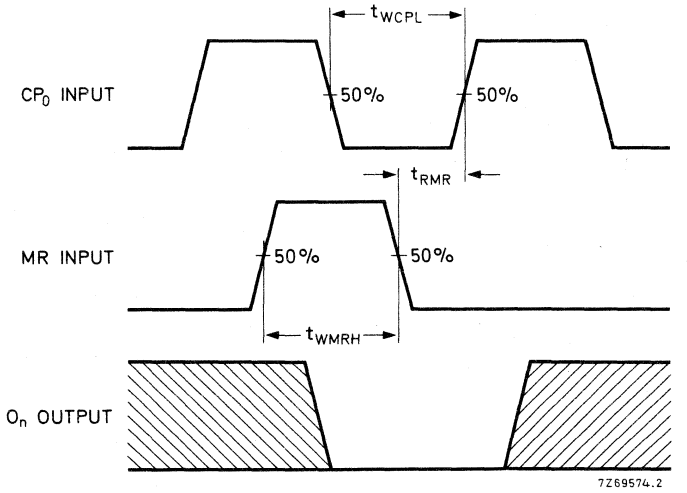
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Hold times	5		140	70		ns	
$CP_0 \rightarrow \overline{CP}_1$	10	t_{hold}	50	25		ns	
	15		30	15		ns	
	5		170	85		ns	
$\overline{CP}_1 \rightarrow CP_0$	10	t_{hold}	60	30		ns	
	15		40	20		ns	
Minimum clock pulse width	5		75	35		ns	
	10	t_{WCP}	30	15		ns	
	15		20	10		ns	see also waveforms on page 5
Minimum MR pulse width; HIGH	5		70	35		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		30	10		ns	
	10	t_{RMR}	15	5		ns	
	15		10	5		ns	
Maximum clock pulse frequency	5		3	6		MHz	
	10	f_{max}	8	16		MHz	
	15		12	24		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6525\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



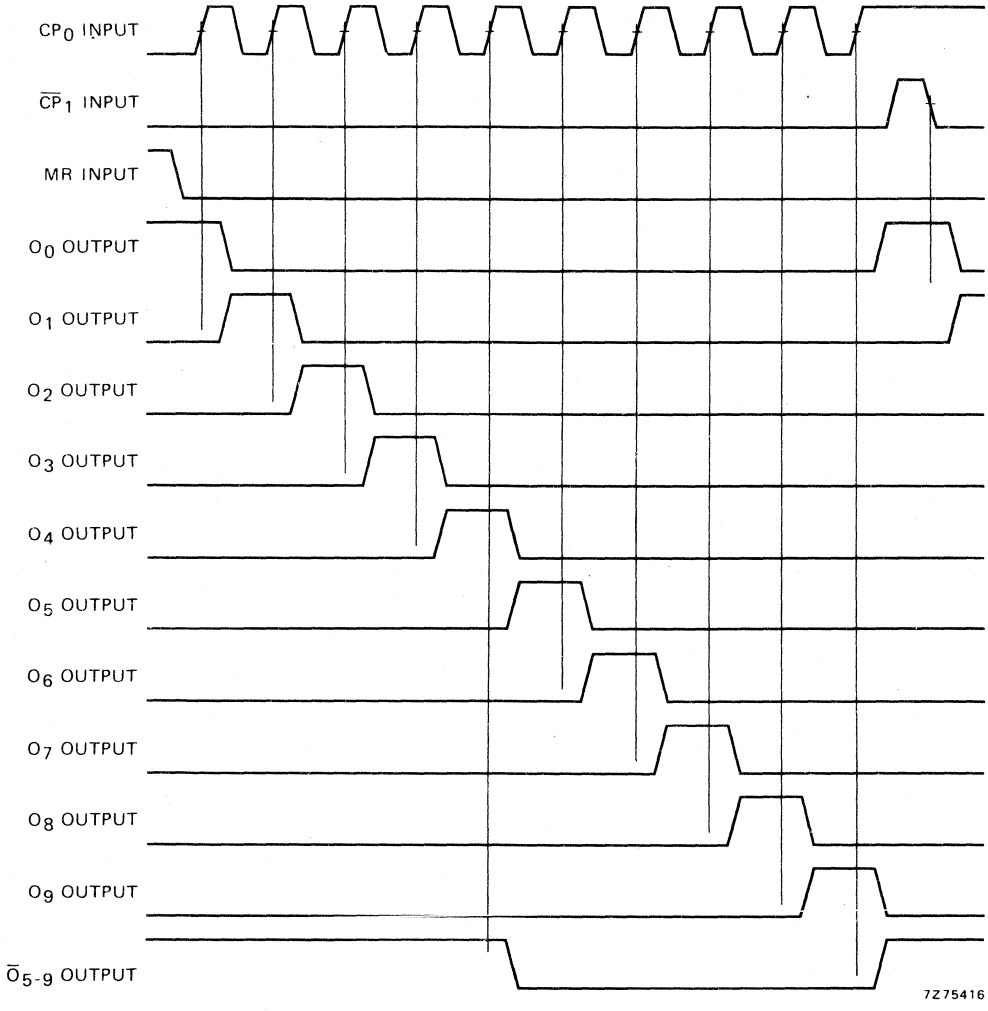
Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.
Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

FUNCTIONAL WAVEFORMS

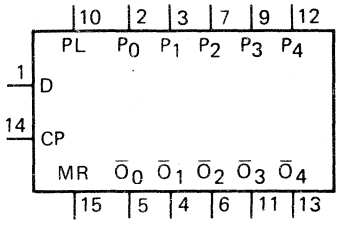


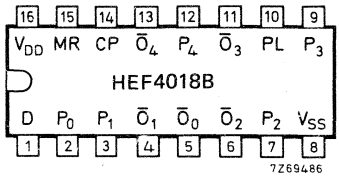
PRESETTABLE DIVIDE-BY-N COUNTER

The HEF4018B is a 5-stage Johnson counter with a clock input (CP), a data input (D), an asynchronous parallel load input (PL), five parallel inputs (P_0 to P_4), five active LOW buffered outputs ($\overline{O}_0$ to $\overline{O}_4$), and an overriding asynchronous master reset input (MR). Information on P_0 to P_4 is asynchronously loaded into the counter while PL is HIGH, independent of CP and D inputs.

Data present in the counter is stored on the HIGH to LOW transition of PL. When PL is LOW, the counter advances on the LOW to HIGH transition of CP. By connecting $\overline{O}_0$ to $\overline{O}_4$ to D, the counter operates as a divide-by-n counter (n = 2 to 10; see also divide-by-n mode selection below).

A HIGH on MR resets the counter ($\overline{O}_0$ to $\overline{O}_4$ = HIGH) independent of all other inputs.





HEF4018BP : 16-lead DIL; plastic (SOT-38Z).
HEF4018BD: 16-lead DIL; ceramic (SOT-74).

DIVIDE-BY-N MODE SELECTION

divide by	D input
2	$\overline{O}_0$
3	$\overline{O}_0 \cdot \overline{O}_1$
4	$\overline{O}_1$
5	$\overline{O}_1 \cdot \overline{O}_2$
6	$\overline{O}_2$
7	$\overline{O}_2 \cdot \overline{O}_3$
8	$\overline{O}_3$
9	$\overline{O}_3 \cdot \overline{O}_4$
10	$\overline{O}_4$

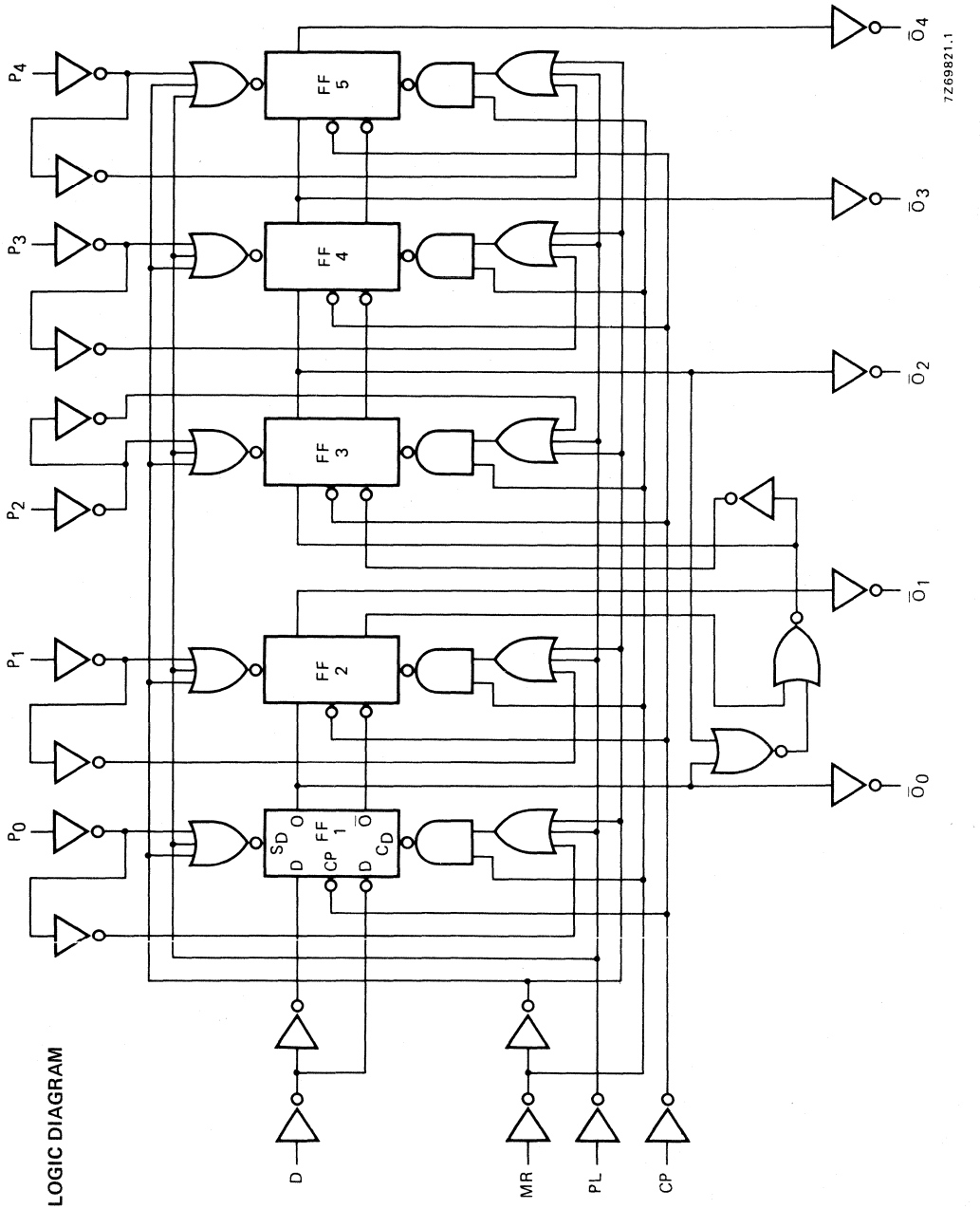
PINNING

PL	parallel load input
P_0 to P_4	parallel inputs
D	data input
CP	clock input (LOW to HIGH edge triggered)
MR	master reset input
$\overline{O}_0$ to $\overline{O}_4$	buffered output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



LOGIC DIAGRAM

A.C. CHARACTERISTICS

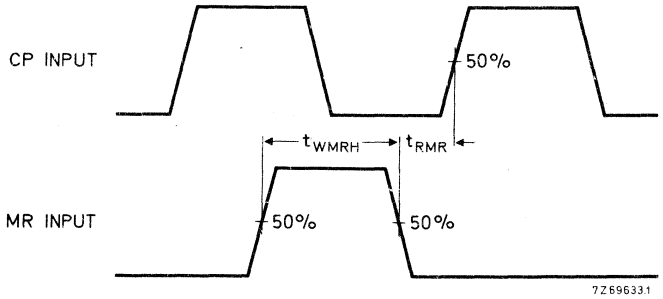
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → $\overline{O}$	5			185	370	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	95	ns	42 ns + (0,16 ns/pF) C_L
	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
PL → $\overline{O}$	5			205	415	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			50	95	ns	42 ns + (0,16 ns/pF) C_L
MR → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
Set-up time	5		130	65		ns	
D → CP	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time	5		20	−45		ns	
D → CP	10	t_{hold}	5	−15		ns	
	15		5	−10		ns	
Minimum clock	5		140	70		ns	
pulse width; LOW	10	t_{WCPL}	50	25		ns	
	15		40	20		ns	
Minimum MR pulse	5		100	50		ns	see also waveforms on pages 4 and 5
width; HIGH	10	t_{WMRH}	35	20		ns	
	15		25	15		ns	
Minimum PL pulse	5		145	75		ns	
width; HIGH	10	t_{WPLH}	50	25		ns	
	15		35	20		ns	
Recovery time	5		135	70		ns	
for MR	10	t_{RMR}	40	20		ns	
	15		25	15		ns	
Recovery time	5		170	85		ns	
for PL	10	t_{RPL}	55	30		ns	
	15		40	20		ns	
Maximum clock	5		2	4		MHz	
pulse frequency	10	f_{max}	6	11		MHz	
	15		8	16		MHz	

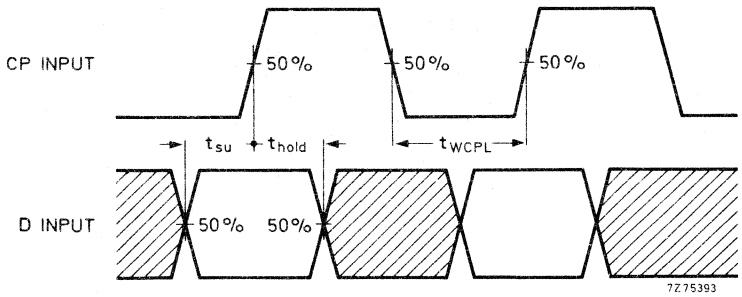
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

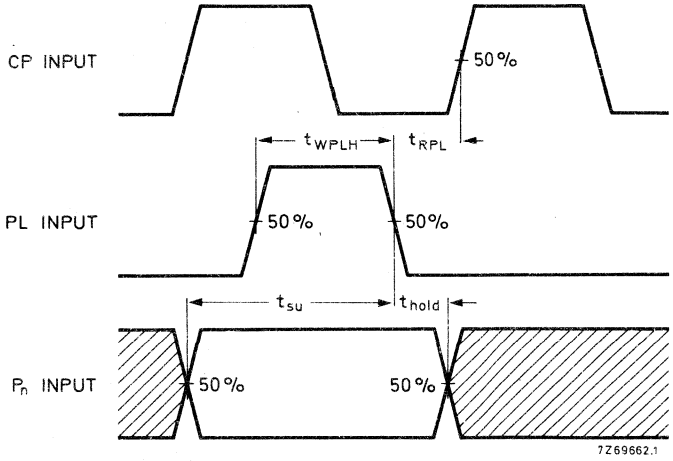
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3450\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing minimum MR pulse width and MR recovery time.

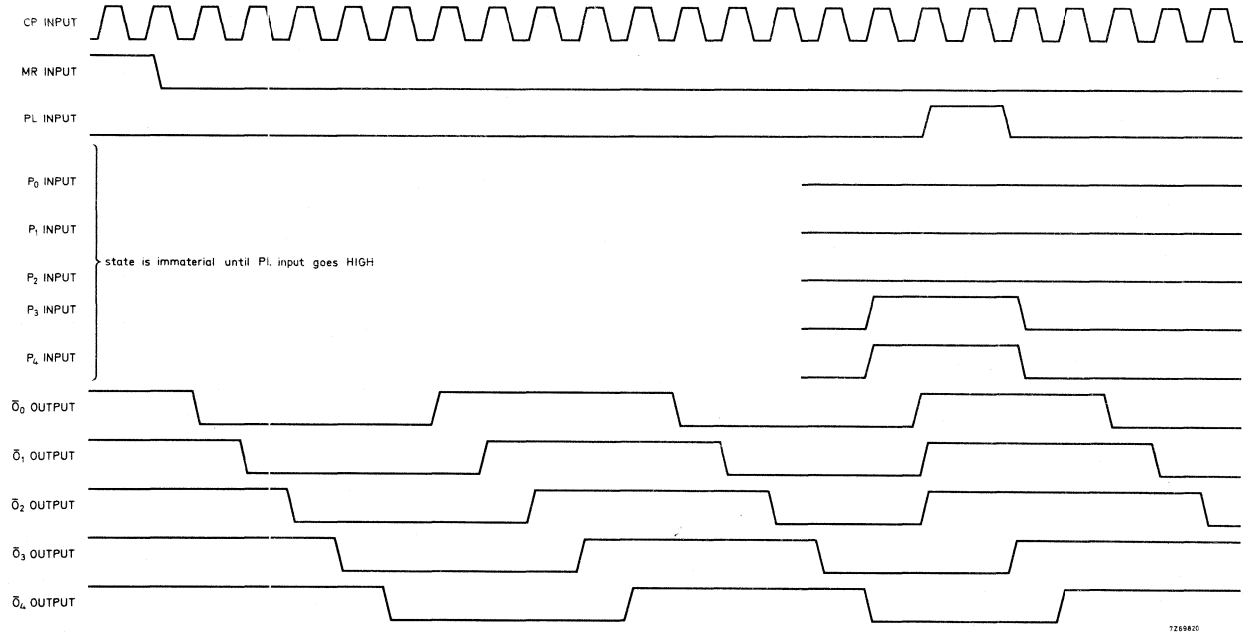


Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D.



Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

TIMING DIAGRAM



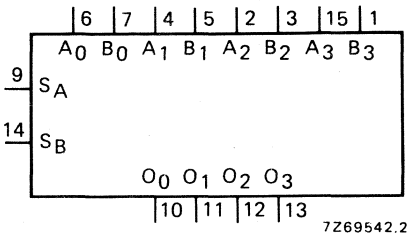
Note

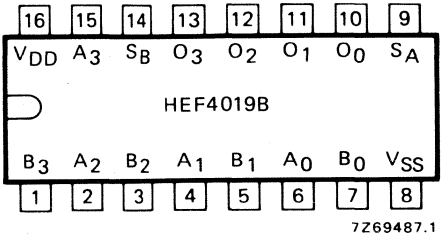
D input connected to $\overline{O}_4$ for decade counter configuration.

QUADRUPLE 2-INPUT MULTIPLEXER

The HEF4019B provides four multiplexing circuits with common select inputs (S_A, S_B); each circuit contains two inputs (A_n, B_n) and one output (O_n). It may be used to select four bits of information from one of two sources.

The A inputs are selected when S_A is HIGH, the B inputs when S_B is HIGH. When S_A and S_B are HIGH, output (O_n) is the logical OR of the A_n and B_n inputs ($O_n = A_n + B_n$). When S_A and S_B are LOW, output (O_n) is LOW independent of the multiplexer inputs.





HEF4019BP: 16-lead DIL; plastic (SOT-38Z).
HEF4019BD: 16-lead DIL; ceramic (SOT-74).

PINNING

S_A, S_B	select inputs (active HIGH)	B_0 to B_3	multiplexer inputs
A_0 to A_3	multiplexer inputs	O_0 to O_3	multiplexer outputs

TRUTH TABLE

select		inputs		output
S_A	S_B	A_n	B_n	O_n
L	L	X	X	L
H	L	L	X	L
H	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	H	H	X	H
H	H	X	H	H
H	H	L	L	L

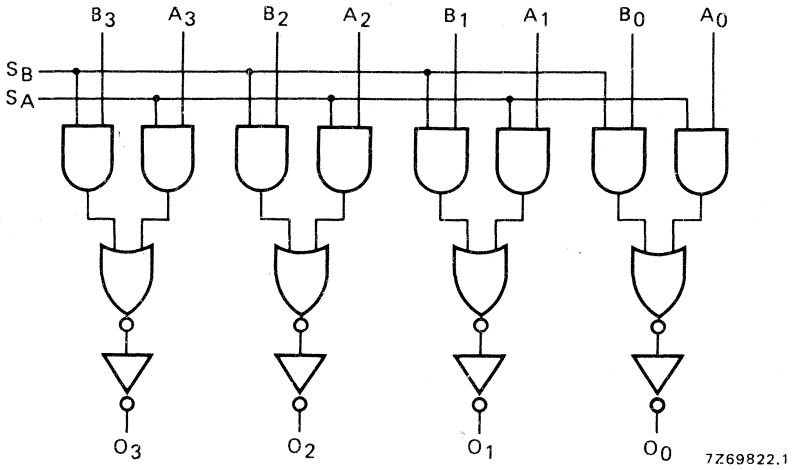
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



A.C. CHARACTERISTICS

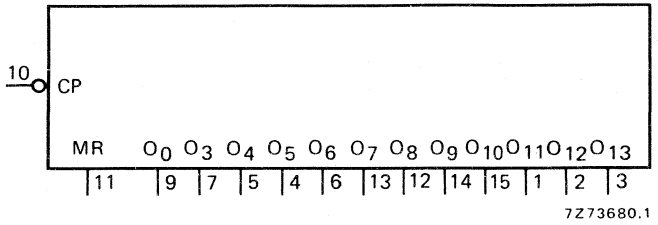
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

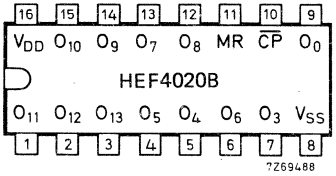
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, B_n, S_A, S_B → O_n	5		70	145	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
	5		60	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	35	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1200 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5100 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	18 700 f_i + Σ($f_o C_L$) x V_{DD}^2	

14-STAGE BINARY COUNTER

The HEF4020B is a 14-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0, O_3 to O_{13}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$.





HEF4020BP: 16-lead DIL; plastic (SOT-38Z).
HEF4020BD: 16-lead DIL; ceramic (SOT-74).

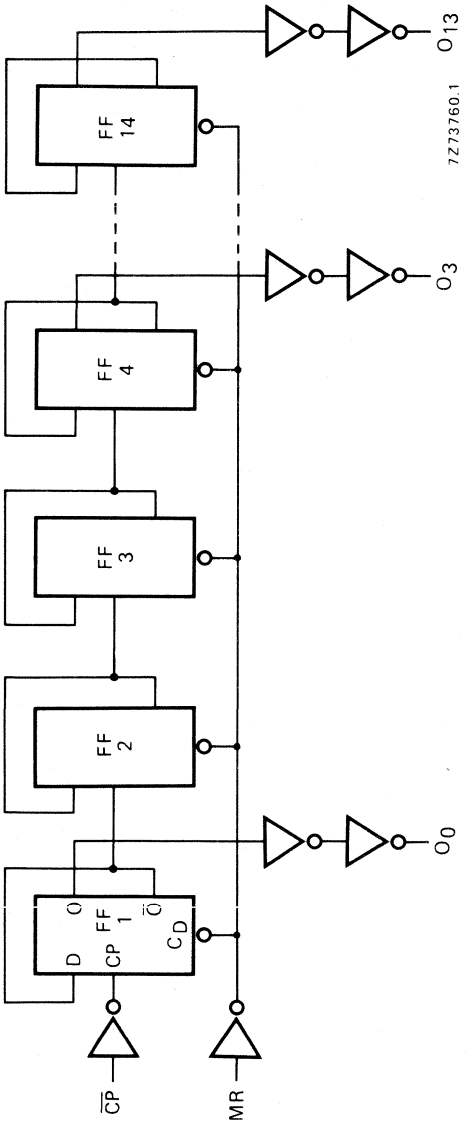
PINNING

$\overline{CP}$	clock input (HIGH to LOW edge triggered)
MR	master reset input (active HIGH)
O_0, O_3 to O_{13}	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM

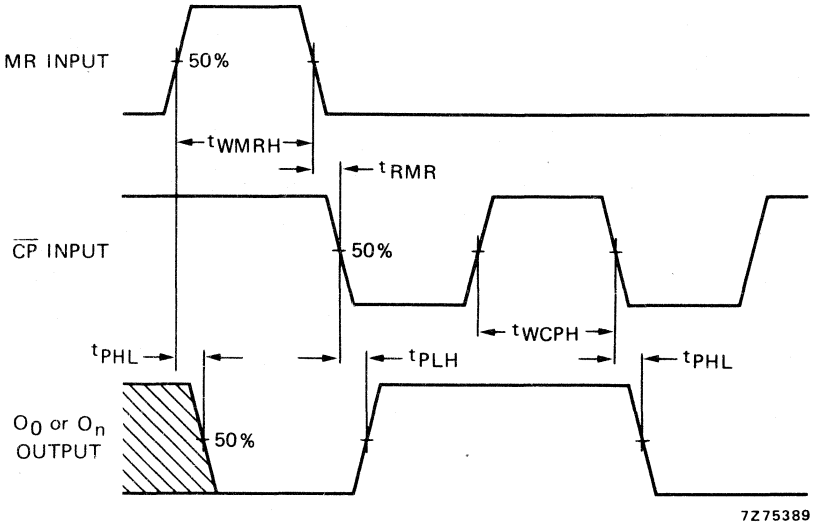


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
$\overline{CP} \longrightarrow O_0$	5			105	210 ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90 ns	34 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
	5			105	210 ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	95 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
$MR \longrightarrow O_n$	5			180	360 ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180 ns	79 ns + (0,23 ns/pF) C_L
	15			70	140 ns	62 ns + (0,16 ns/pF) C_L
Minimum clock	5		50	25	ns	
pulse width; HIGH	10	t_{WCPH}	25	15	ns	
	15		20	10	ns	
Minimum MR	5		130	65	ns	
pulse width; HIGH	10	t_{WMRH}	95	50	ns	
	15		90	45	ns	see also waveforms on page 4
Recovery time	5		115	60	ns	
for MR	10	t_{RMR}	65	35	ns	
	15		55	25	ns	
Maximum clock	5		5	10	MHz	
pulse frequency	10	f_{max}	13	25	MHz	
	15		18	35	MHz	

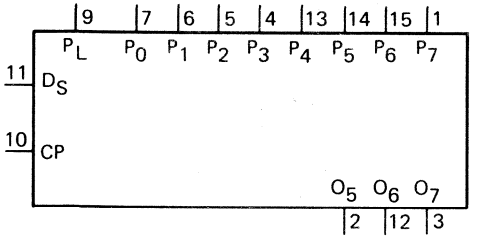
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	8200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

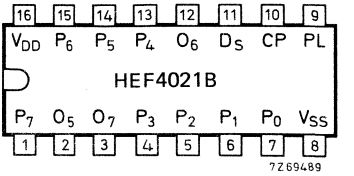


Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.

8-BIT STATIC SHIFT REGISTER

The HEF4021B is an edge-triggered 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (D_S), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (P_0 to P_7) and buffered parallel outputs from the last three stages (O_5 to O_7). Information on P_0 to P_7 is asynchronously loaded into the register while PL is HIGH, independent of CP and D_S. When PL is LOW, data on D_S is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP.





HEF4021BP: 16-lead DIL; plastic (SOT-38Z).
HEF4021BD: 16-lead DIL; ceramic (SOT-74).

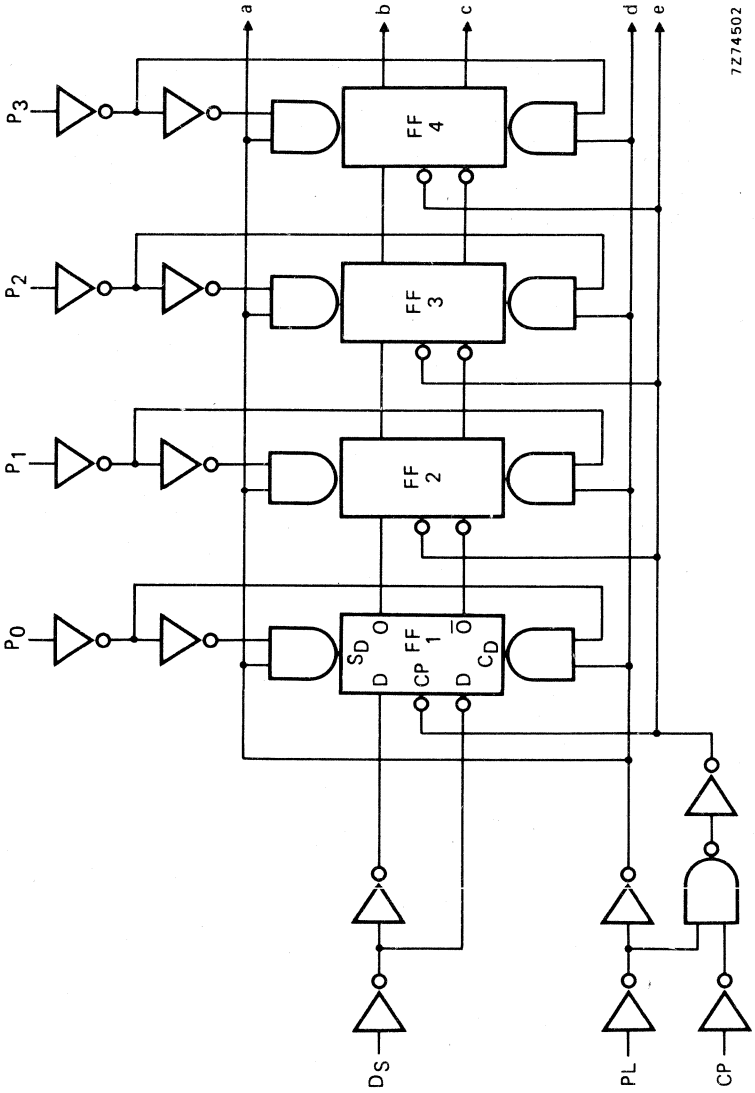
PINNING

PL	parallel load input
P_0 to P_7	parallel data inputs
D_S	serial data input
CP	clock input (LOW to HIGH edge-triggered)
O_5 to O_7	buffered parallel outputs from the last three stages

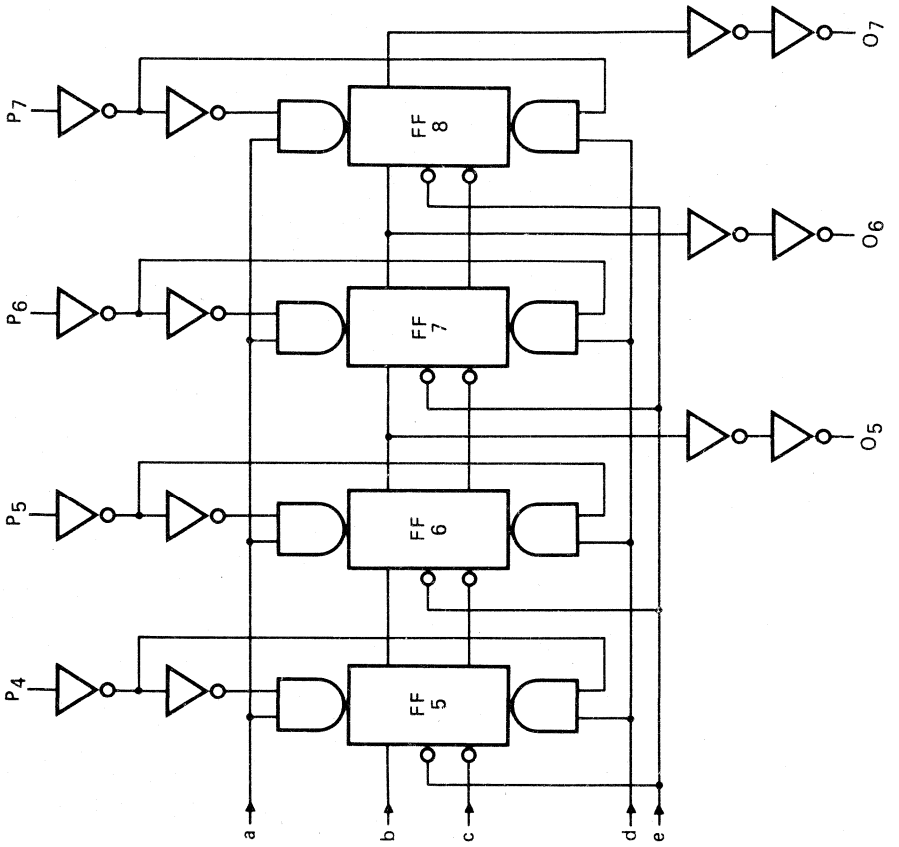
FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



TRUTH TABLES

Serial operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
1	∫	D_1	L	X	X	X
2	∫	D_2	L	X	X	X
3	∫	D_3	L	X	X	X
6	∫	X	L	D_1	X	X
7	∫	X	L	D_2	D_1	X
8	∫	X	L	D_3	D_2	D_1
	⌝	X	L	no change		

Parallel operation

	inputs			outputs		
n	CP	D_S	PL	O_5	O_6	O_7
	X	X	H	P_5	P_6	P_7

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			170	340	ns	143 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF)C_L
	15			45	90	ns	37 ns + (0,16 ns/pF)C_L
	5			130	260	ns	103 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF)C_L
	15			40	80	ns	32 ns + (0,16 ns/pF)C_L
PL → O_n	5			240	480	ns	213 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF)C_L
	15			60	125	ns	52 ns + (0,16 ns/pF)C_L
	5			175	355	ns	148 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF)C_L
	15			50	100	ns	42 ns + (0,16 ns/pF)C_L
Set-up times	5		90	45		ns	
D_S → CP	10	t_{su}	35	15		ns	
	15		25	10		ns	
	5		145	70		ns	
P_n → PL	10	t_{su}	55	25		ns	
	15		40	20		ns	
Hold times	5		20	−25		ns	
D_S → CP	10	t_{hold}	10	−10		ns	
	15		10	−5		ns	
	5		20	−55		ns	
P_n → PL	10	t_{hold}	10	−10		ns	
	15		10	−10		ns	

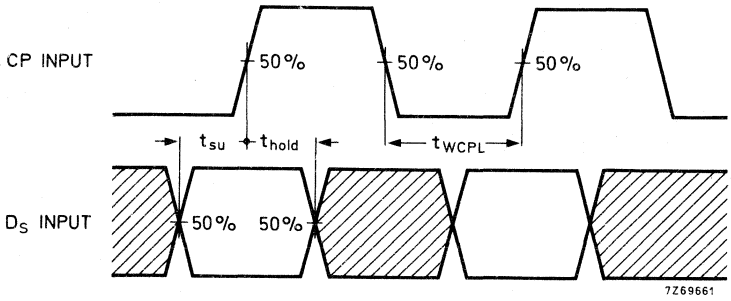
see also waveforms on page 6

A.C. CHARACTERISTICS

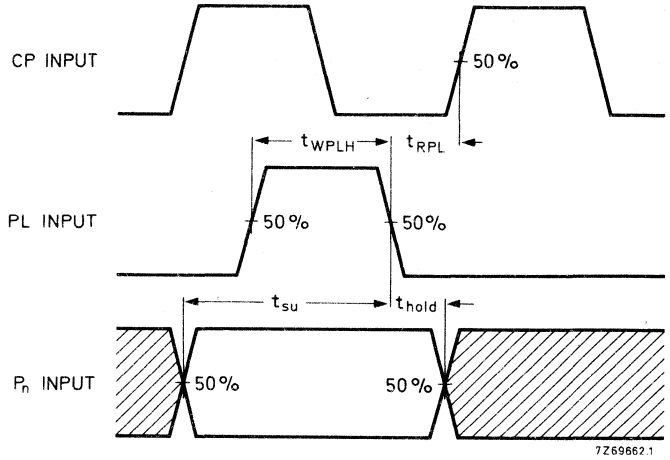
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55	ns	see also waveforms on page 6
	10		40	20	ns	
	15		30	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	150	75	ns	
	10		55	25	ns	
	15		40	20	ns	
Recovery time for PL	5	t_{RPL}	120	60	ns	
	10		40	20	ns	
	15		30	15	ns	
Maximum clock pulse frequency	5	f_{max}	4	9	MHz	
	10		12	25	MHz	
	15		18	37	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5250\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,250\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing minimum clock pulse width, set-up time and hold time for CP and D_S.



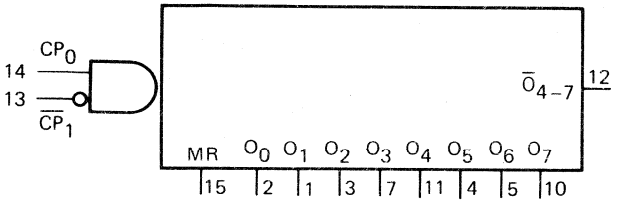
Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

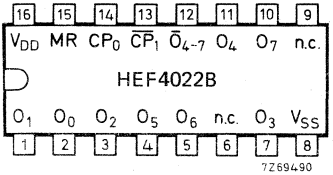
4-STAGE DIVIDE-BY-8 JOHNSON COUNTER

The HEF4022B is a 4-stage divide-by-8 Johnson counter with eight spike-free decoded active HIGH outputs (O_0 to O_7), an active LOW output from the most significant flip-flop ($\overline{O}_{4-7}$), active HIGH and active LOW clock inputs (CP_0, $\overline{CP}_1$) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while $\overline{CP}_1$ is LOW or a HIGH to LOW transition at $\overline{CP}_1$ while CP_0 is HIGH (see also function table on page 3). When cascading counters, the $\overline{O}_{4-7}$ output, which is LOW while the counter is in states 4, 5, 6 and 7, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \overline{O}_{4-7}$ = HIGH; O_1 to O_7 = LOW) independent of the clock inputs (CP_0, $\overline{CP}_1$).





HEF4022BP : 16-lead DIL; plastic (SOT-38Z).
HEF4022BD: 16-lead DIL; ceramic (SOT-74).

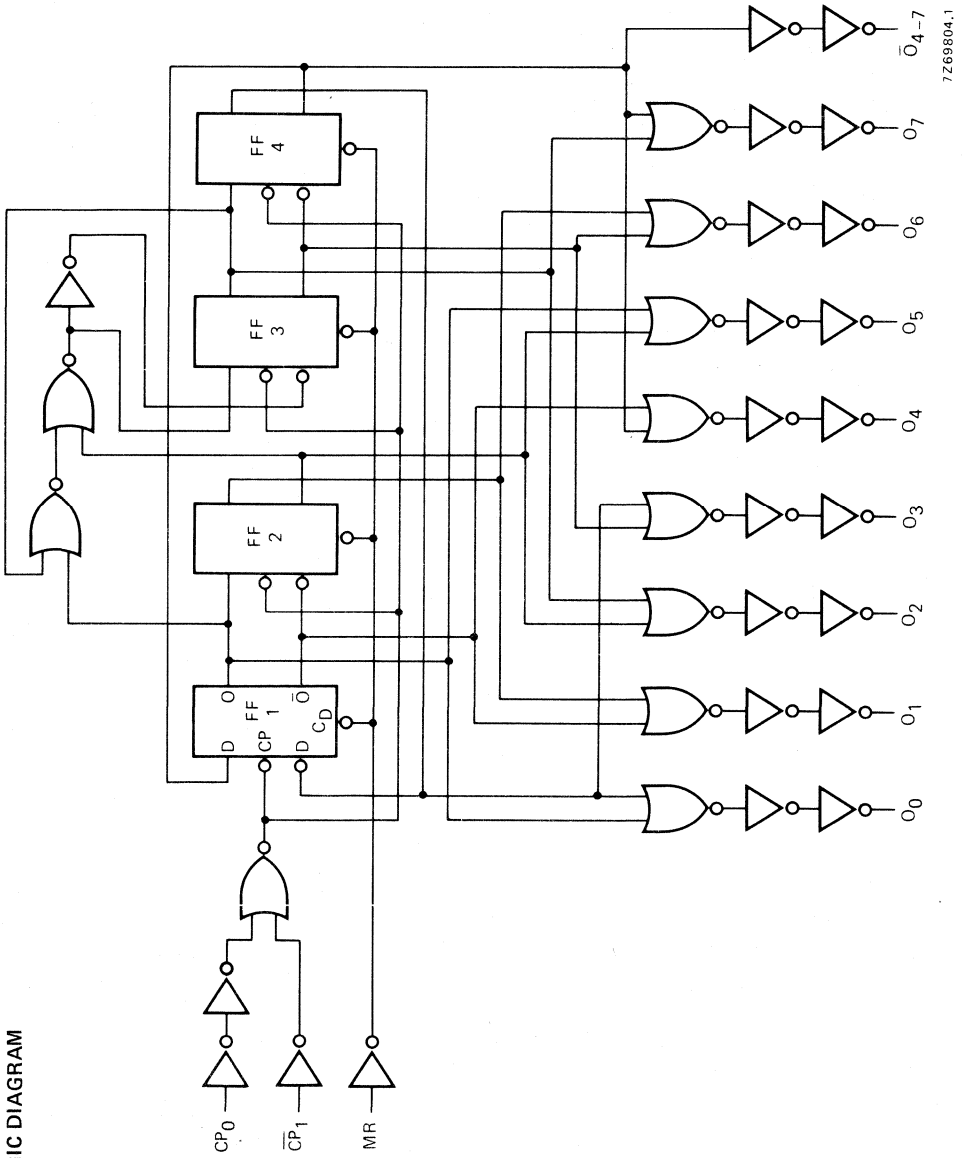
PINNING

CP_0	clock input (LOW to HIGH; edge-triggered)
$\overline{CP}_1$	clock input (HIGH to LOW; edge-triggered)
MR	master reset input
O_0 to O_7	decoded outputs
$\overline{O}_{4-7}$	carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

MR	CP_0	$\overline{CP}_1$	operation
H	X	X	$O_0 = \overline{O}_{4-7} = H$; O_1 to $O_7 = L$
L	H	⟍	Counter advances
L	⨍	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	⨍	No change
L	⟍	L	No change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⨍ = positive-going transition
⟍ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

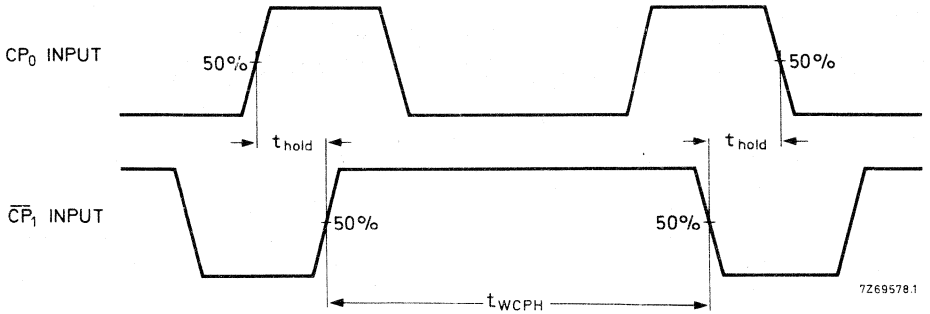
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP_0, $\overline{CP}_1$ → O_n	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		95	195	ns	84 ns + (0,23 ns/pF) C_L
	15			60	125	ns	52 ns + (0,16 ns/pF) C_L
CP_0, $\overline{CP}_1$ → $\overline{O}_{4-7}$	5			245	485	ns	218 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	185	ns	79 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			190	380	ns	163 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	145	ns	64 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
MR → $\overline{O}_{4-7}$	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

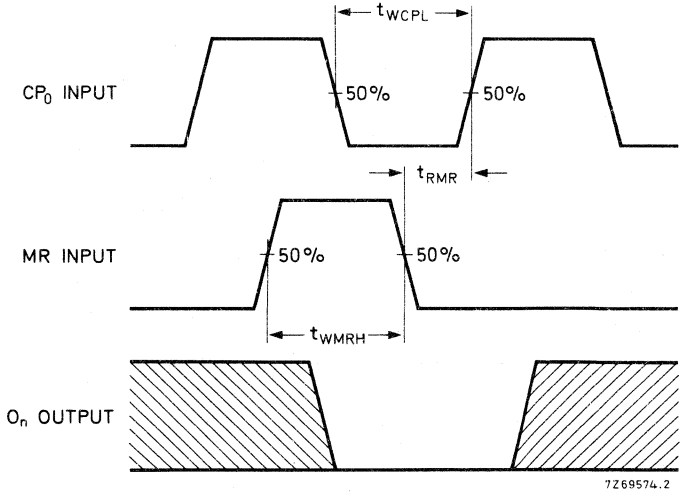
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Hold times	5		140	70	ns	see also waveforms on page 5
$CP_0 \rightarrow \overline{CP}_1$	10	t_{hold}	50	25	ns	
	15		30	15	ns	
	5		170	85	ns	
$\overline{CP}_1 \rightarrow CP_0$	10	t_{hold}	60	30	ns	
	15		40	20	ns	
Minimum clock pulse width	5		75	35	ns	
	10	t_{WCP}	30	15	ns	
	15		20	10	ns	
Minimum MR pulse width; HIGH	5		70	35	ns	
	10	t_{WMRH}	30	15	ns	
	15		20	10	ns	
Recovery time for MR	5		30	10	ns	
	10	t_{RMR}	15	5	ns	
	15		10	5	ns	
Maximum clock pulse frequency	5		3	6	MHz	
	10	f_{max}	8	16	MHz	
	15		12	24	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$475\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



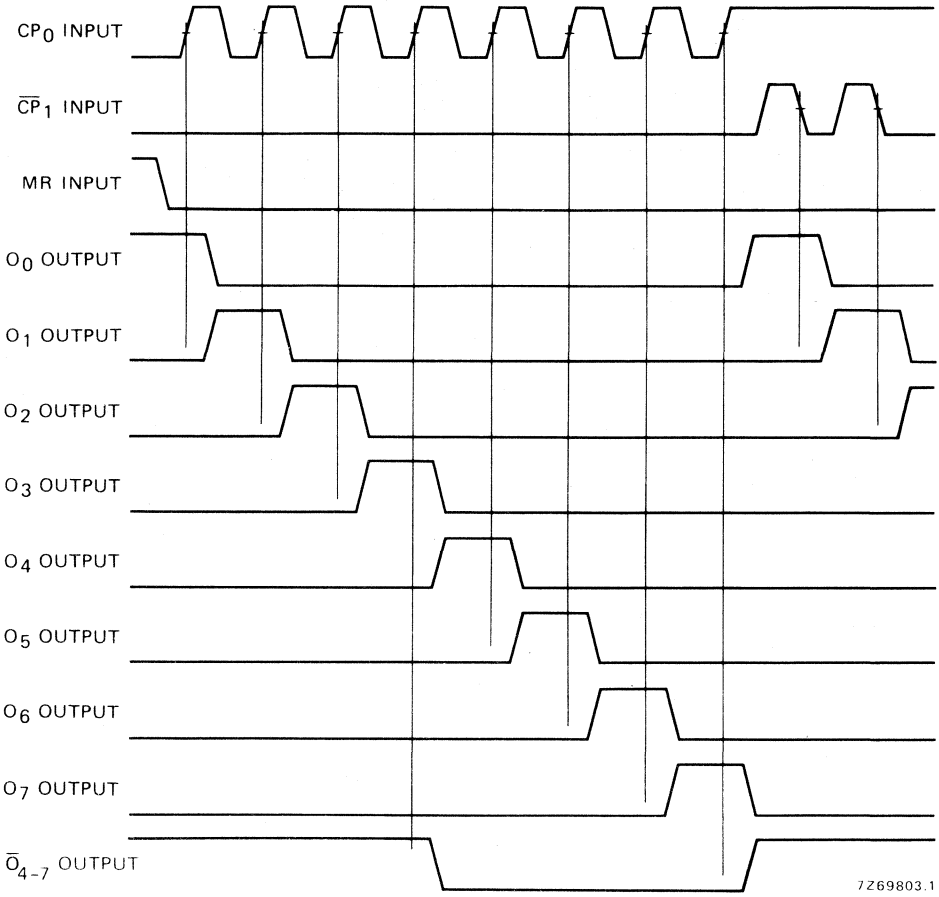
Waveforms showing hold times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0.
Hold times are shown as positive values, but may be specified as negative values.



Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths.

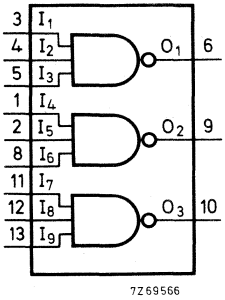
Conditions: $\overline{CP}_1$ = LOW while CP_0 is triggered on a LOW to HIGH transition.
t_{WCP} and t_{RMR} also apply when CP_0 = HIGH and $\overline{CP}_1$ is triggered on a HIGH to LOW transition.

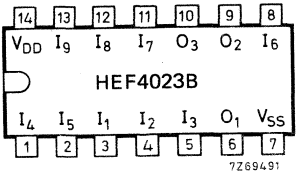
FUNCTIONAL WAVEFORMS



TRIPLE 3-INPUT NAND GATE

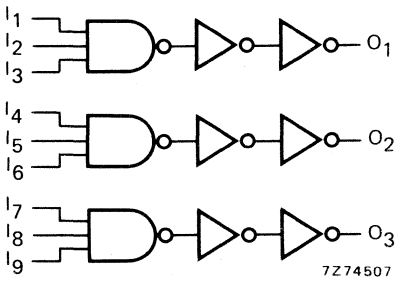
The HEF4023B provides the positive triple 3-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4023BP : 14-lead DIL; plastic (SOT-27).
HEF4023BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

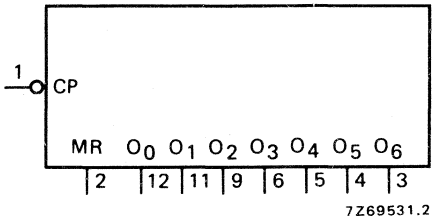
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

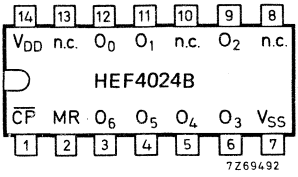
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		65	135	ns	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	45	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

7-STAGE BINARY COUNTER

The HEF4024B is a 7-stage binary ripple counter with a clock input ($\overline{CP}$), and overriding asynchronous master reset input (MR) and seven fully buffered parallel outputs (O_0 to O_6). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$.





HEF4024BP: 14-lead DIL; plastic (SOT-27).
HEF4024BD: 14-lead DIL; ceramic (SOT-73).

PINNING

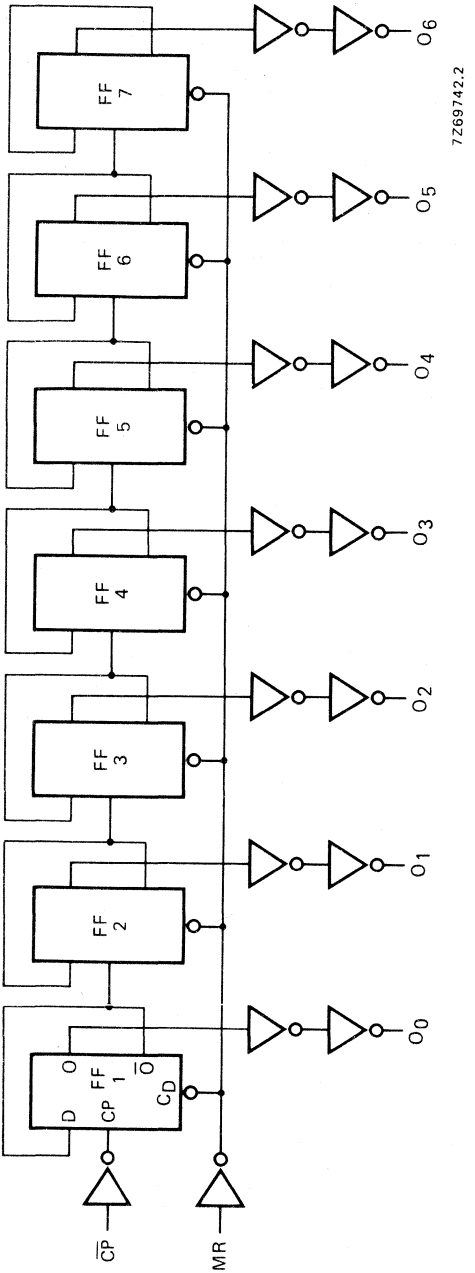
$\overline{CP}$	clock input (HIGH to LOW triggered)
MR	master reset input
O_0 to O_6	buffered parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM

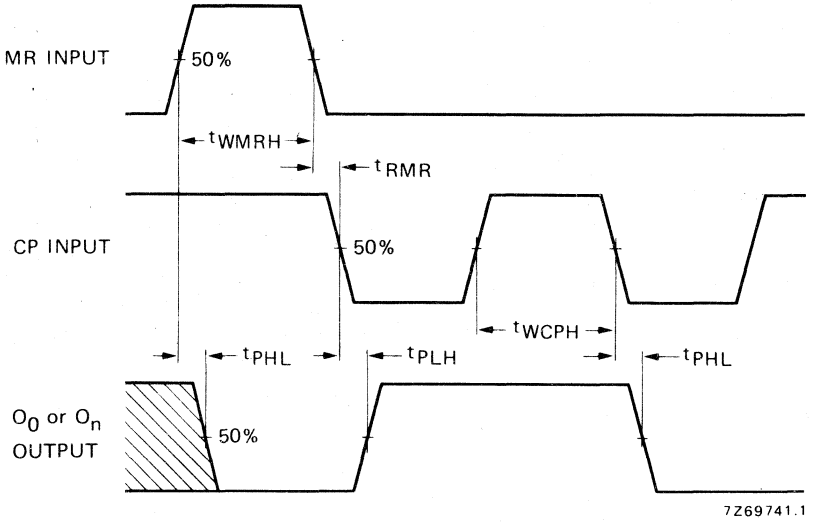


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{CP} \longrightarrow O_0$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	75	ns	29 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	85	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$MR \longrightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Minimum clock	5		60	30		ns	
pulse width; HIGH	10	t_{WCPH}	30	15		ns	
	15		20	10		ns	
Minimum MR	5		80	40		ns	
pulse width; HIGH	10	t_{WMRH}	35	20		ns	
	15		25	15		ns	see also waveforms on page 4
Recovery time	5		20	10		ns	
for MR	10	t_{RMR}	15	5		ns	
	15		15	5		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

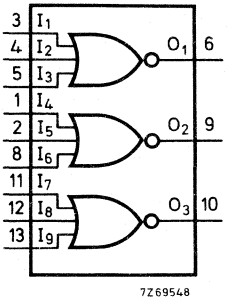
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

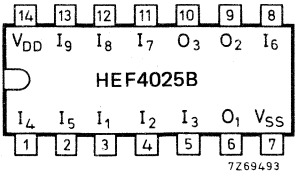


Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths and recovery time for MR.

TRIPLE 3-INPUT NOR GATE

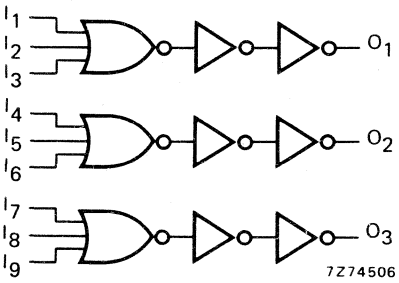
The HEF4025B provides the positive triple 3-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4025BP : 14-lead DIL; plastic (SOT-27).
HEF4025BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA
I_{DD} LIMITS category GATES
} see Family Specifications

A.C. CHARACTERISTICS

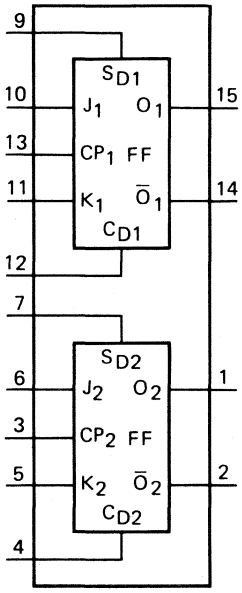
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		70	135	ns	43 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	55	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		15	35	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL JK FLIP-FLOP

The HEF4027B is a dual JK flip-flop which is edge-triggered and features independent set direct, clear direct, and clock inputs. Data are accepted when CP is LOW and transferred to the output on the positive-going edge of the clock. The active HIGH asynchronous clear-direct (C_D) and set-direct (S_D) are independent and override the J, K and CP inputs. The outputs are buffered for best system performance.



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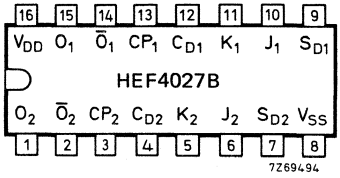


7Z69494

HEF4027BP : 16-lead DIL; plastic (SOT-38Z).
HEF4027BD: 16-lead DIL; ceramic (SOT-74).

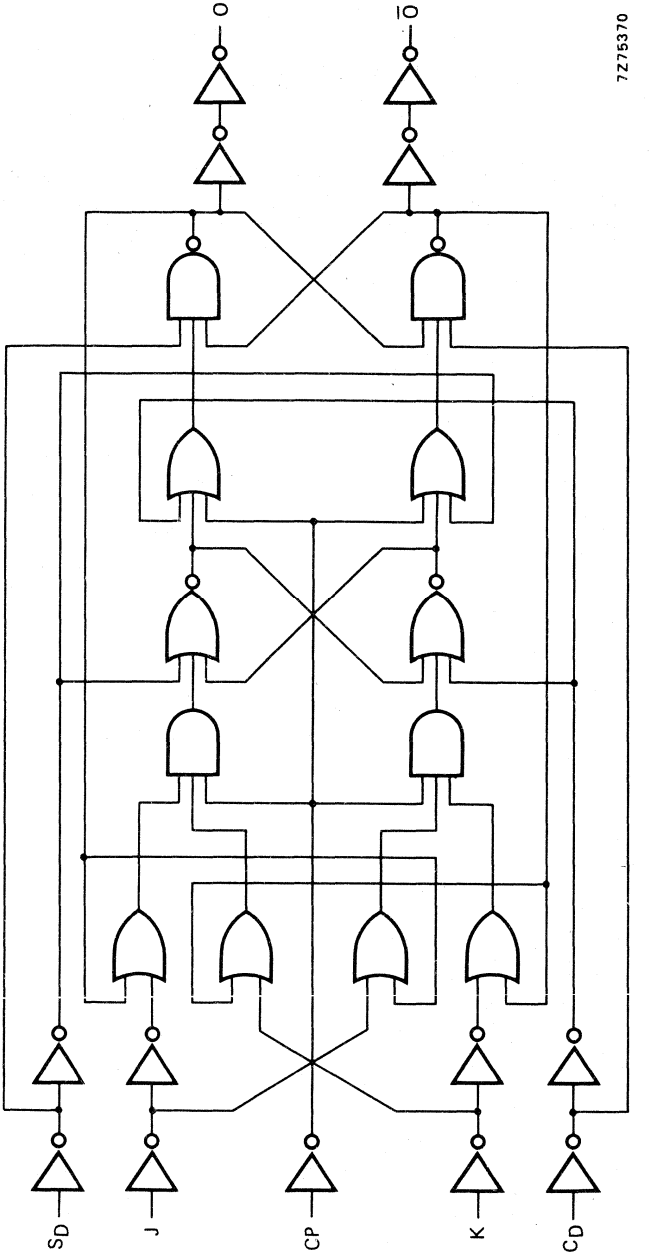
PINNING

J, K synchronous inputs
CP clock input (LOW to HIGH edge-triggered)
S_D asynchronous set-direct input (active HIGH)
C_D asynchronous clear-direct input (active HIGH)
O true output
$\overline{O}$ complement output

FAMILY DATA

I_{DD} **LIMITS category FLIP-FLOPS** } see Family Specifications

LOGIC DIAGRAM (one flip-flop)



TRUTH TABLES

inputs					outputs	
S_D	C_D	CP	J	K	O_{n+1}	$\overline{O}_{n+1}$
L	L	∫	L	L	no change	
L	L	∫	H	L	H	L
L	L	∫	L	H	L	H
L	L	∫	H	H	$\overline{O}_n$	O_n

inputs					outputs	
S_D	C_D	CP	J	K	O	$\overline{O}$
H	L	X	X	X	H	L
L	H	X	X	X	L	H
H	H	X	X	X	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
O_{n+1} = state after clock positive transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O, $\overline{O}$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
S_D → O	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	45	ns	17 ns + (0,16 ns/pF) C_L
C_D → O	5			130	260	ns	102 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
Set-up time	5		95	50		ns	
J, K → CP	10	t_{su}	30	15		ns	
	15		20	10		ns	
Hold time	5		15	−30		ns	
J, K → CP	10	t_{hold}	10	−5		ns	
	15		10	0		ns	
Minimum clock	5		95	50		ns	
pulse width; LOW	10	t_{WCPL}	40	20		ns	
	15		30	15		ns	
Minimum S_D, C_D	5		80	40		ns	
pulse width; HIGH	10	t_{WSDH}, t_{WCDH}	40	20		ns	
	15		30	15		ns	
Recovery time	5		40	10		ns	
for S_D, C_D	10	t_{RSD}, t_{RCD}	25	5		ns	
	15		15	0		ns	

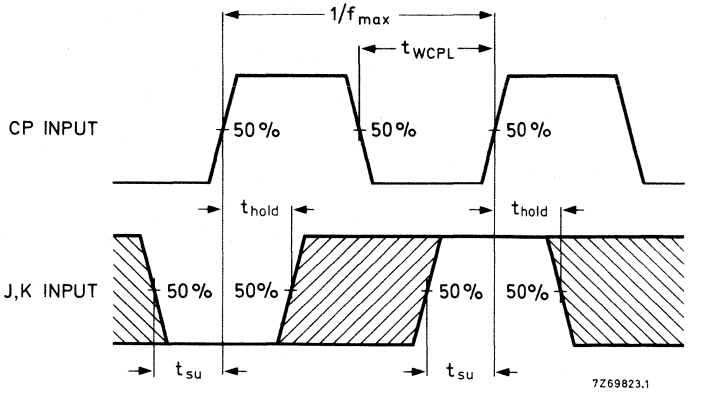
see also waveforms on page 5

A.C. CHARACTERISTICS

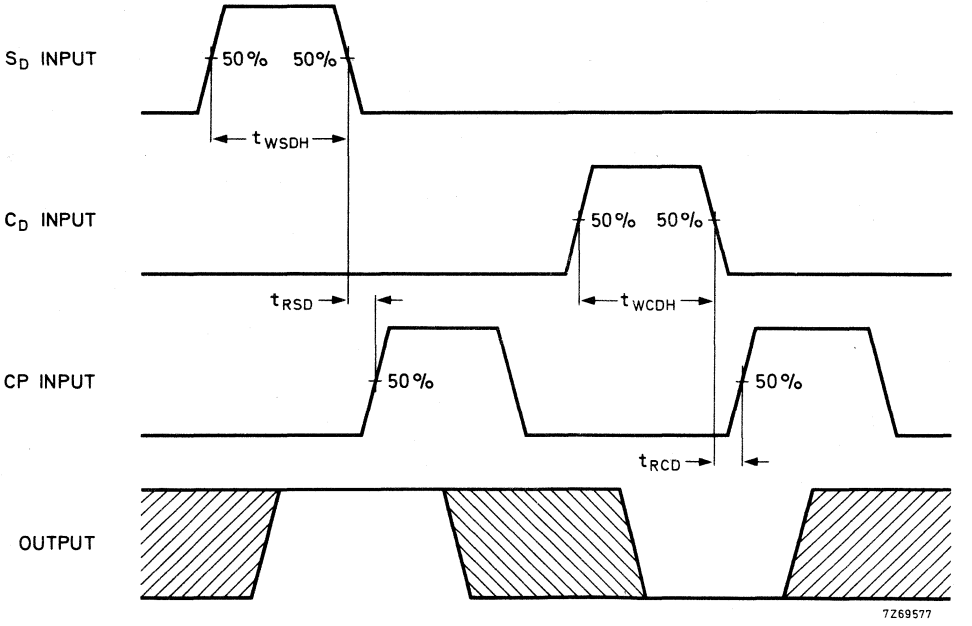
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Maximum clock pulse frequency J = K = HIGH	5	f_{max}	3	6	MHz	see also waveforms on page 5
	10		7	15	MHz	
	15		11	22	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



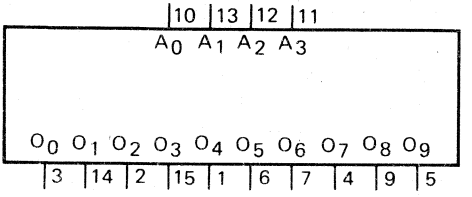
Waveforms showing set-up times, hold times and minimum clock pulse width.



Waveforms showing recovery times for S_D and C_D; minimum S_D and C_D pulse widths.
Set-up times and hold times are shown as positive values but may be specified as negative values.

1-OF-10 DECODER

The HEF4028B is a 4-bit BCD to 1-of-10 active HIGH decoder. A 1-2-4-8 BCD code applied to inputs A_0 to A_3 causes the selected output to be HIGH, the other nine will be LOW. If desired, the device may be used as a 1-of-8 decoder with enable; 3-bit octal inputs are applied to inputs A_0, A_1 and A_2 selecting an output O_0 to O_7. Input A_3 then becomes an active LOW enable, forcing the selected output LOW when A_3 is HIGH. The HEF4028B may also be used as an 8-input demultiplexer with an active LOW data input. The outputs are fully buffered for best performance.



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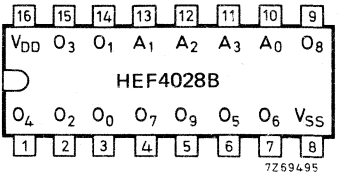


7Z69495

HEF4028BP: 16-lead DIL; plastic (SOT-38Z).
HEF4028BD: 16-lead DIL; ceramic (SOT-74).

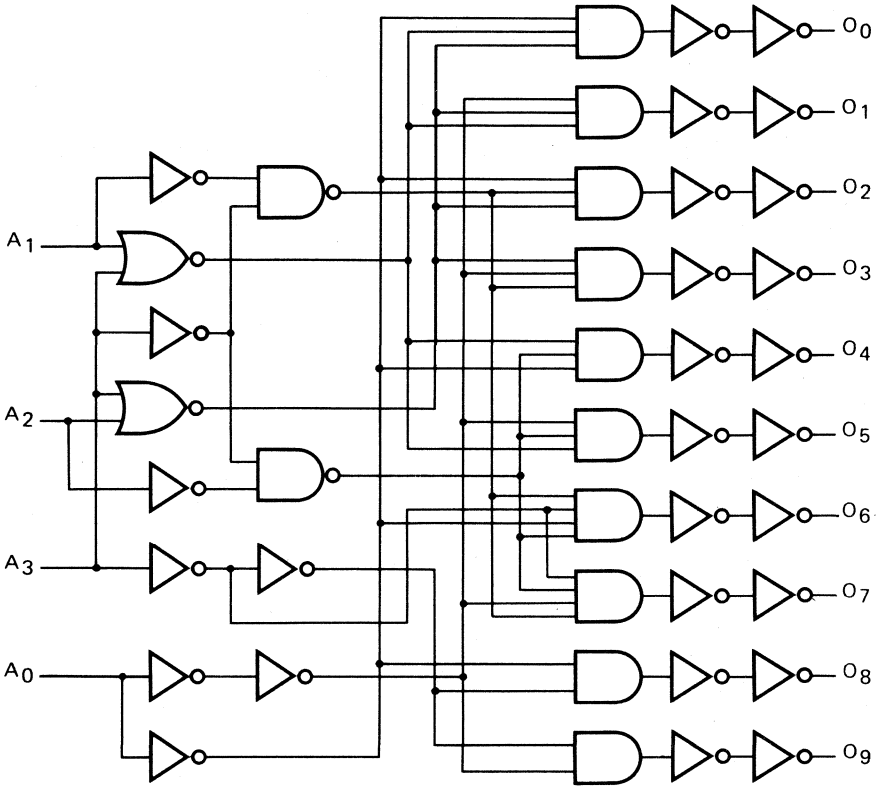
PINNING

A_0 to A_3	address inputs, 1-2-4-8 BCD
O_0 to O_9	outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

inputs				outputs									
A_3	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	
L	L	L	L	H	L	L	L	L	L	L	L	L	L	
L	L	L	H	L	H	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
L	H	L	L	L	L	L	L	H	L	L	L	L	L	
L	H	L	H	L	L	L	L	L	H	L	L	L	L	
L	H	H	L	L	L	L	L	L	L	H	L	L	L	
L	H	H	H	L	L	L	L	L	L	L	H	L	L	
H	L	L	L	L	L	L	L	L	L	L	L	H	L	
H	L	L	H	L	L	L	L	L	L	L	L	L	H	
H	L	H	L	L	L	L	L	L	L	L	L	H	L	*
H	L	H	H	L	L	L	L	L	L	L	L	L	H	*
H	H	L	L	L	L	L	L	L	L	L	L	H	L	*
H	H	L	H	L	L	L	L	L	L	L	L	L	H	*
H	H	H	L	L	L	L	L	L	L	L	L	H	L	*
H	H	H	H	L	L	L	L	L	L	L	L	L	H	*

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

* Extraordinary states.

A.C. CHARACTERISTICS

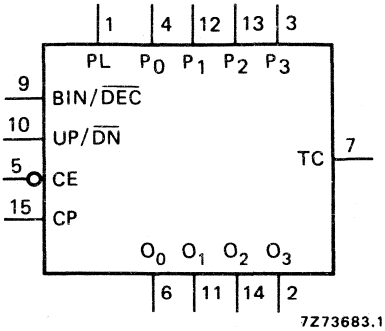
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

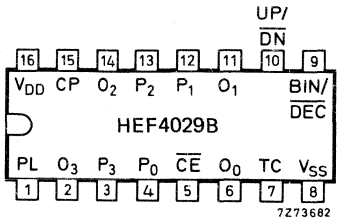
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$A_n \rightarrow O_n$	5		110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	95	ns	39 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
	5		100	195	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	45	85	ns	34 ns + (0,23 ns/pF) C_L
	15		30	65	ns	22 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	7500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	20 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

SYNCHRONOUS UP/DOWN COUNTER, BINARY/DECADE COUNTER

The HEF4029B is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/$\overline{DN}$), a binary/decade control input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output (TC).





HEF4029BP : 16-lead DIL; plastic (SOT-38Z).
HEF4029BD: 16-lead DIL; ceramic (SOT-74).

PINNING

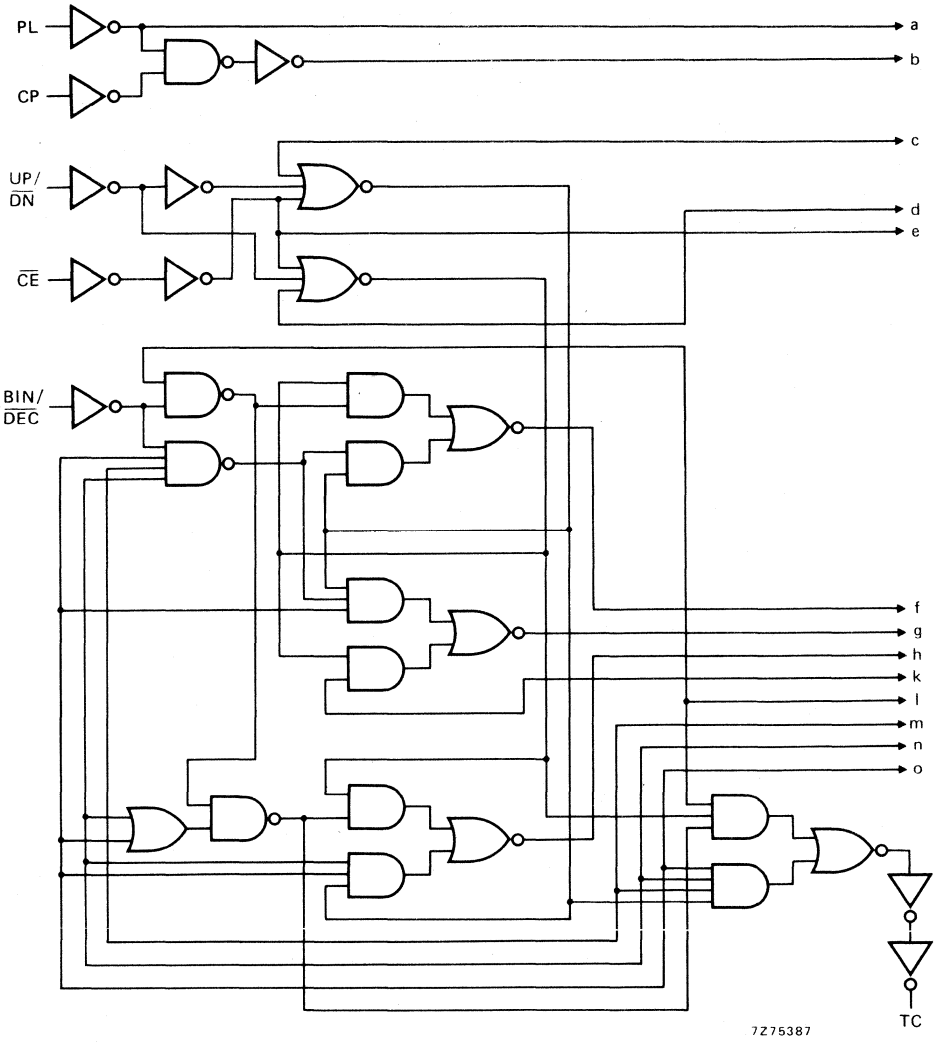
PL	parallel load input
P_0 to P_3	parallel data inputs
BIN/$\overline{DEC}$	binary/decade control input
UP/$\overline{DN}$	up/down control input
$\overline{CE}$	count enable input (active LOW)
CP	clock input (LOW to HIGH, edge triggered)
O_0 to O_3	buffered parallel outputs
TC	terminal count output (active LOW)

FAMILY DATA

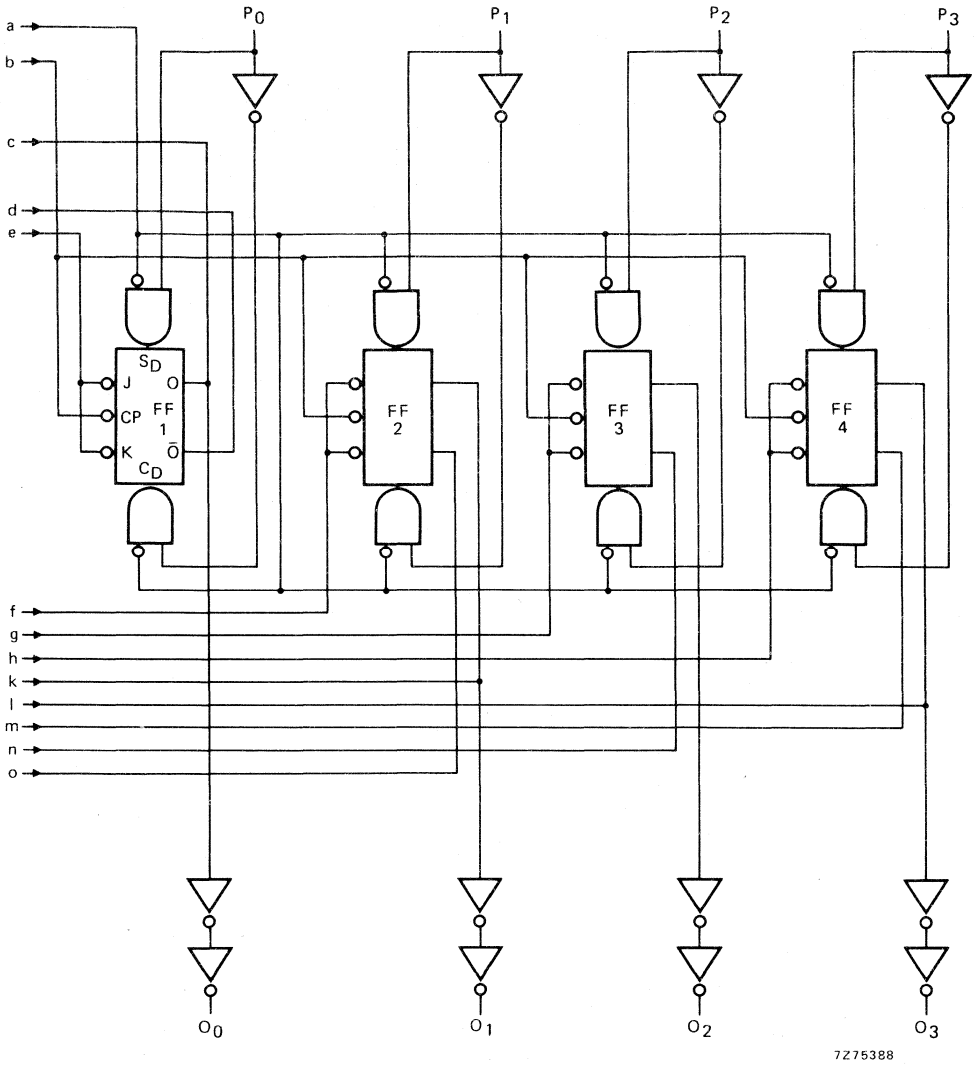
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)

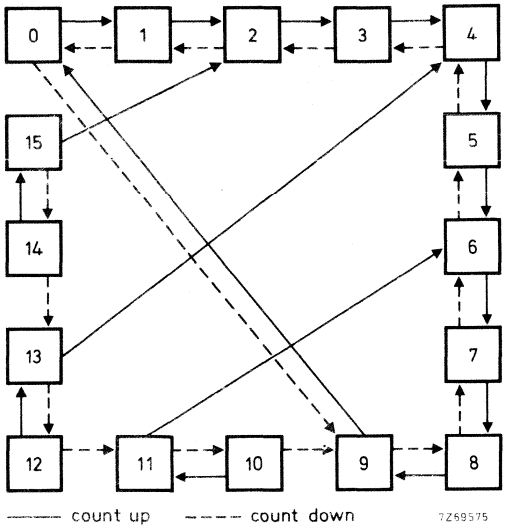


FUNCTION TABLE

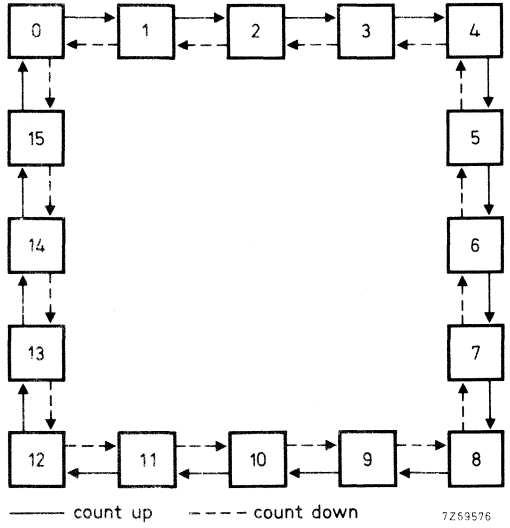
PL	BIN/$\overline{DEC}$	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
H	X	X	X	X	parallel load ($P_n \rightarrow O_n$)
L	X	X	H	X	no change
L	L	L	L	⎍	count-down, decade
L	L	H	L	⎍	count-up, decade
L	H	L	L	⎍	count-down, binary
L	H	H	L	⎍	count-up, binary

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going clock pulse edge

STATE DIAGRAM: BIN/$\overline{DEC}$ = LOW



STATE DIAGRAM: BIN/$\overline{DEC}$ = HIGH



Logic equation for terminal count:

$$TC = \overline{\overline{CE}\,(BIN/\overline{DEC}\cdot UP/\overline{DN}\cdot O_0\cdot O_1\cdot O_2\cdot O_3 + BIN/\overline{DEC}\cdot \overline{UP/\overline{DN}}\cdot \overline{O}_0\cdot \overline{O}_1\cdot \overline{O}_2\cdot \overline{O}_3 + \overline{BIN/\overline{DEC}}\cdot UP/\overline{DN}\cdot O_0\cdot O_3 + \overline{BIN/\overline{DEC}}\cdot \overline{UP/\overline{DN}}\cdot \overline{O}_0\cdot \overline{O}_1\cdot \overline{O}_2\cdot \overline{O}_3)}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

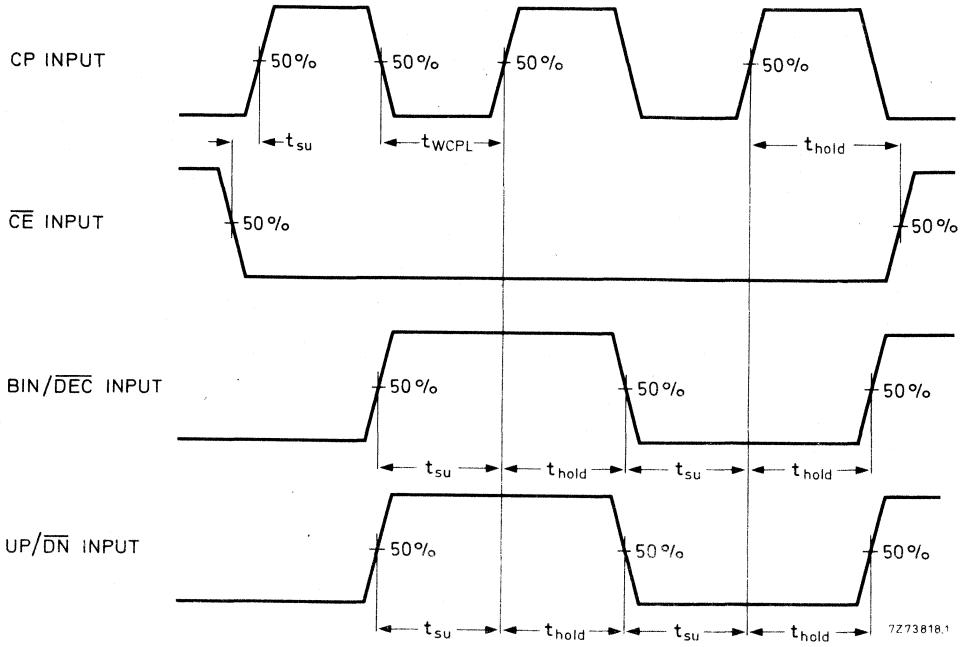
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
	5			160	315	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CP → TC	5			280	560	ns	253 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	205	ns	94 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
	5			195	385	ns	168 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	105	ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			170	335	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → TC	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			170	335	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L

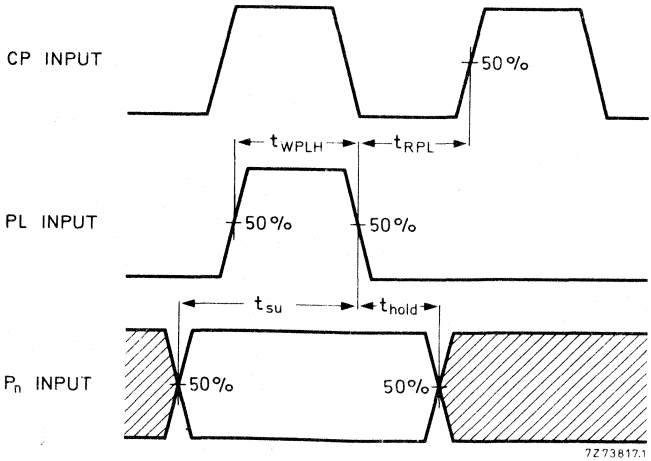
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	110	55		ns	
	10		35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	160	80		ns	
	10		55	25		ns	
	15		35	15		ns	
Recovery time for PL	5	t_{RPL}	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Set-up times BIN/$\overline{DEC}$ → CP	5	t_{su}	270	135		ns	
	10		90	45		ns	
	15		60	30		ns	
UP/$\overline{DN}$ → CP	5	t_{su}	300	150		ns	
	10		105	55		ns	
	15		75	35		ns	
$\overline{CE}$ → CP	5	t_{su}	120	60		ns	
	10		45	25		ns	
	15		35	20		ns	see also waveforms on page 8
P_n → PL	5	t_{su}	70	35		ns	
	10		20	10		ns	
	15		10	5		ns	
Hold times BIN/$\overline{DEC}$ → CP	5	t_{hold}	45	−90		ns	
	10		15	−30		ns	
	15		10	−20		ns	
UP/$\overline{DN}$ → CP	5	t_{hold}	15	−135		ns	
	10		0	−50		ns	
	15		−5	−35		ns	
$\overline{CE}$ → CP	5	t_{hold}	30	−30		ns	
	10		10	−10		ns	
	15		5	−10		ns	
P_n → PL	5	t_{hold}	15	−20		ns	
	10		0	−10		ns	
	15		0	−5		ns	
Maximum clock pulse frequency	5	f_{max}	4	8		MHz	
	10		12	25		MHz	
	15		18	35		MHz	



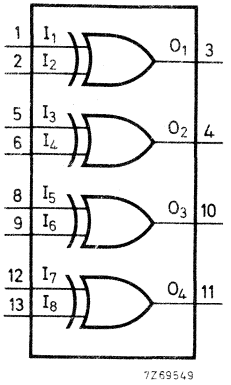
Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP, BIN/$\overline{DEC}$ to CP and UP/$\overline{DN}$ to CP. Set-up and hold times are shown as positive values but may be specified as negative values.



Waveforms showing minimum pulse width for PL, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE EXCLUSIVE-OR GATE

The HEF4030B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



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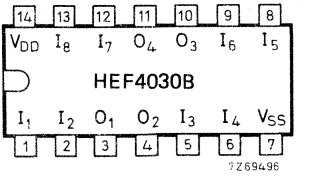

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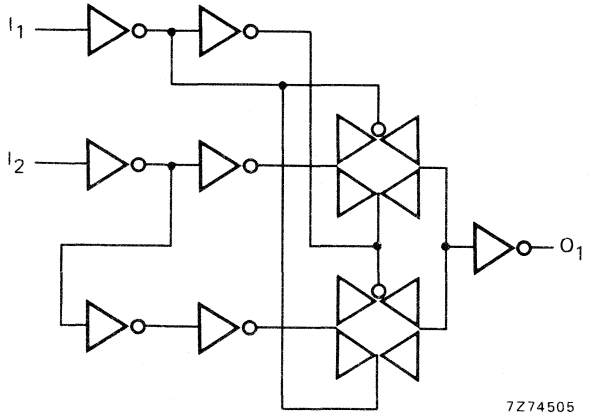
HEF4030BP : 14-lead DIL; plastic (SOT-27).
HEF4030BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



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TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specification

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

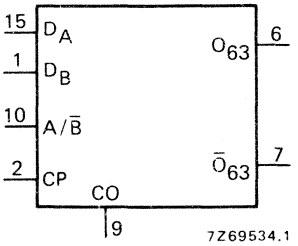
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		85	175	ns	57 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	75	ns	23 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	47 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

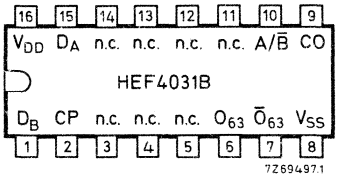
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

64-STAGE STATIC SHIFT REGISTER

The HEF4031B is an edge-triggered 64-stage static shift register with two serial data inputs (D_A, D_B), a data select input $A/\overline{B}$, a clock input (CP), a buffered clock output (CO), and buffered outputs from the 64th bit position (O_{63}, $\overline{O}_{63}$). The output O_{63} is capable of driving one TTL load.

Data from D_A or D_B, as determined by the state of $A/\overline{B}$, is shifted into the first shift register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D_A is selected by a HIGH, and D_B by a LOW on $A/\overline{B}$. Registers can be cascaded either by connecting all CP inputs together or by driving CP of the most right-hand register with the system clock and connecting CO to CP of the preceding register. When the second technique is used in the recirculating mode, a flip-flop must be used to store O_{63} of the most right-hand register until the most left-hand register is clocked.





HEF4031BP : 16-lead DIL; plastic (SOT-38Z).
HEF4031BD: 16-lead DIL; ceramic (SOT-74).

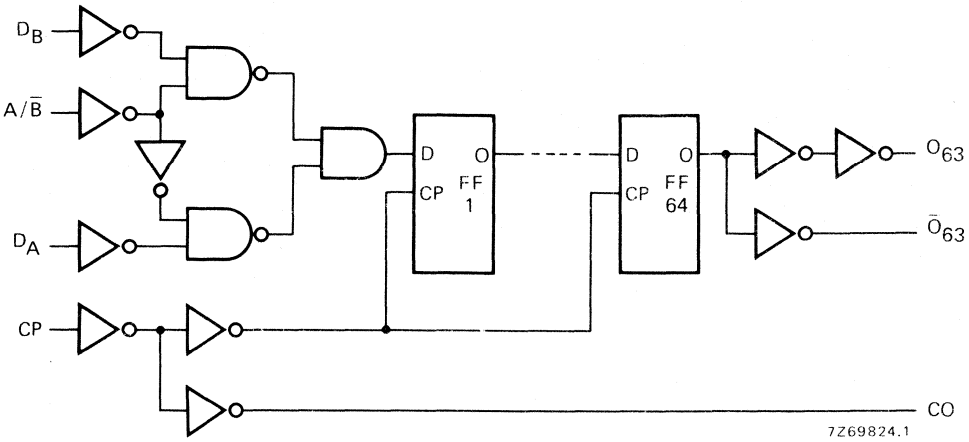
PINNING

D_A, D_B	data inputs
$A/\overline{B}$	data select input
CP	clock input (LOW to HIGH edge-triggered)
CO	buffered clock output
O_{63}	buffered output from the 64th stage
$\overline{O}_{63}$	complementary buffered output from the 64th stage

FAMILY DATA see Family Specifications.

I_{DD} LIMITS category LSI see page 2.

LOGIC DIAGRAM



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Quiescent device current	5	I_{DD}		50		50		375	μA
	10			100		100		750	μA
	15			200		200		1500	μA

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current HIGH; O_{63}	5	4,6		$-I_{OH}$	1,0		0,85		0,65		mA
	10	9,5			3,0		2,5		2,0		mA
	15	13,5			10,0		8,5		6,5		mA
HIGH; O_{63}	5	2,5		$-I_{OH}$	3,0		2,5		2,0		mA
Output current LOW; O_{63}	4,75		0,4	I_{OL}	2,7		2,3		1,8		mA
	10		0,5		9,5		8,0		6,3		mA
	15		1,5		24,0		20,0		16,0		mA

DEVELOPMENT SAMPLE DATA

A.C. CHARACTERISTICS

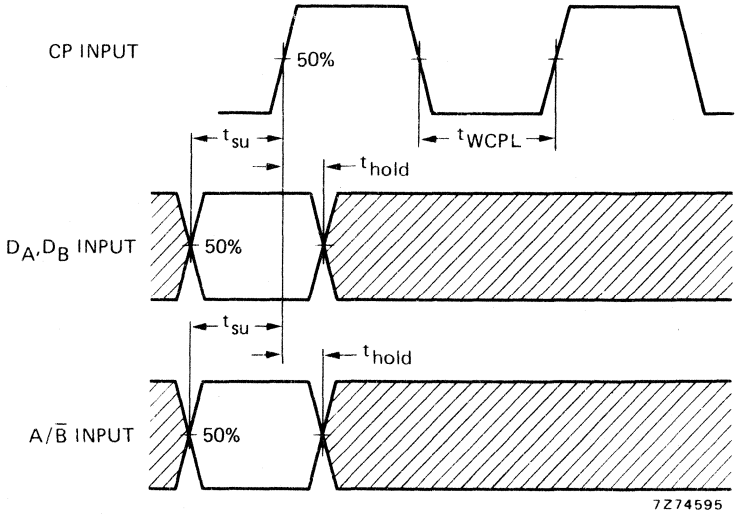
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP → O_{63}	5			240	ns	227 ns + (0,26 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	ns	77 ns + (0,16 ns/pF) C_L
	15			60	ns	54 ns + (0,11 ns/pF) C_L
	5			220	ns	198 ns + (0,45 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	ns	71 ns + (0,19 ns/pF) C_L
	15			55	ns	49 ns + (0,13 ns/pF) C_L
CP → $\overline{O}_{63}$	5			240	ns	213 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	ns	74 ns + (0,23 ns/pF) C_L
	15			60	ns	52 ns + (0,16 ns/pF) C_L
	5			220	ns	193 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	ns	69 ns + (0,23 ns/pF) C_L
	15			55	ns	47 ns + (0,16 ns/pF) C_L
CP → CO	5			80	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	ns	34 ns + (0,23 ns/pF) C_L
	15			40	ns	32 ns + (0,16 ns/pF) C_L
	5			80	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	ns	34 ns + (0,23 ns/pF) C_L
	15			40	ns	32 ns + (0,16 ns/pF) C_L
Transition times; O_{63}	5			35	ns	15 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		17	ns	8 ns + (0,18 ns/pF) C_L
	15			13	ns	7 ns + (0,13 ns/pF) C_L
	5			50	ns	18 ns + (0,65 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		25	ns	10 ns + (0,30 ns/pF) C_L
	15			20	ns	10 ns + (0,20 ns/pF) C_L
Set-up times	5			10	ns	
D_A, D_B → CP	10	t_{su}		5	ns	
	15			0	ns	
	5			10	ns	
A/$\overline{B}$ → CP	10	t_{su}		5	ns	
	15			0	ns	
Hold times	5			0	ns	
D_A, D_B → CP	10	t_{hold}		0	ns	see also waveforms on page 4
	15			0	ns	
	5			0	ns	
A/$\overline{B}$ → CP	10	t_{hold}		0	ns	
	15			0	ns	
Maximum clock	5			5	MHz	
pulse frequency	10	f_{max}		14	MHz	
	15			20	MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$3\,300\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	10	$14\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$35\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	



Waveforms showing minimum clock pulse width, set-up and hold times for D_A, D_B to CP and $A/\overline{B}$ to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT UNIVERSAL SHIFT REGISTER

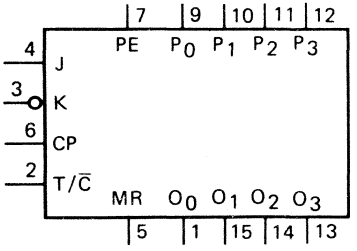
The HEF4035B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input (PE), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a true/complement input ($T/\overline{C}$) and an overriding asynchronous master reset input (MR).

Operation is synchronous (except for MR) and is edge-triggered on the LOW to HIGH transition of the CP input. When PE is HIGH, data is loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP.

When PE is LOW, data is shifted into the first register position from J and $\overline{K}$ and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. D-type entry is obtained by interconnecting J and $\overline{K}$.

The outputs (O_0 to O_3) are either inverting or non-inverting, depending on $T/\overline{C}$ state. With $T/\overline{C}$ HIGH, O_0 to O_3 are non-inverting (active HIGH) and when $T/\overline{C}$ is LOW, O_0 to O_3 are inverting (active LOW).

A HIGH on MR resets all four bit positions (O_0 to O_3 = LOW if $T/\overline{C}$ = HIGH, O_0 to O_3 = HIGH if $T/\overline{C}$ = LOW) independent of all other input conditions.



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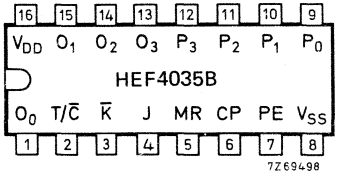


7Z69498

HEF4035BP: 16-lead DIL; plastic (SOT-38Z).
HEF4035BD: 16-lead DIL; ceramic (SOT-74).

PINNING

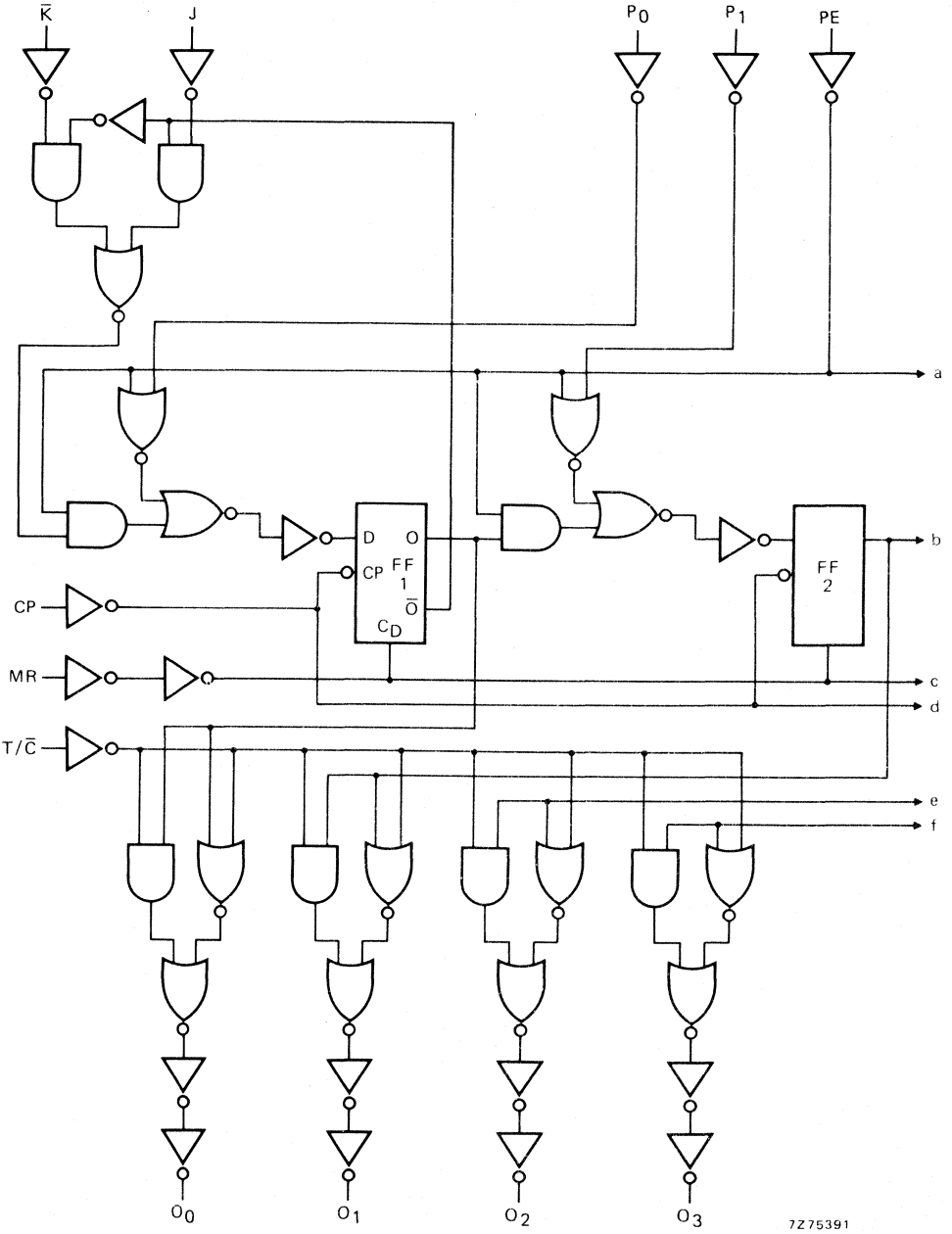
PE	parallel enable input
P_0 to P_3	parallel data inputs
J	first stage J-input (active HIGH)
$\overline{K}$	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge-triggered)
$T/\overline{C}$	true/complement input
MR	master reset input
O_0 to O_3	buffered parallel outputs

FAMILY DATA

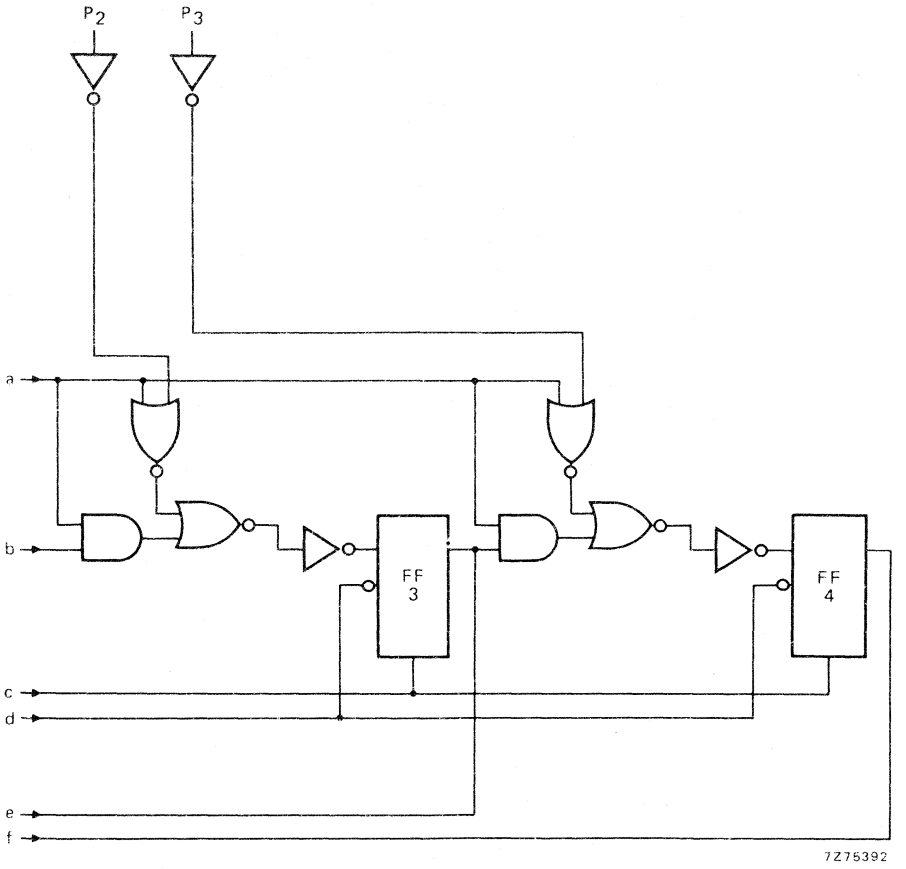
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



TRUTH TABLES

Serial operation

n	inputs				outputs			
	CP	J	$\overline{K}$	MR	O_0	O_1	O_2	O_3
1	∫	L	L	L	L	X	X	X
2	∫	H	H	L	H	L	X	X
3	∫	H	L	L	L	H	L	X
4	∫	H	L	L	H	L	H	L
5	∫	L	H	L	H	H	L	H
	⌝	X	X	L	no change			
	X	X	X	H	L	L	L	L

T/$\overline{C}$ = HIGH; PE = LOW

Parallel operation

CP	inputs				outputs			
	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3
∫	H	H	H	H	H	H	H	H
∫	L	L	L	L	L	L	L	L

T/$\overline{C}$ = HIGH; PE = HIGH; MR = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

n = number of clock pulse transitions
∫ = positive-going transition
⌝ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

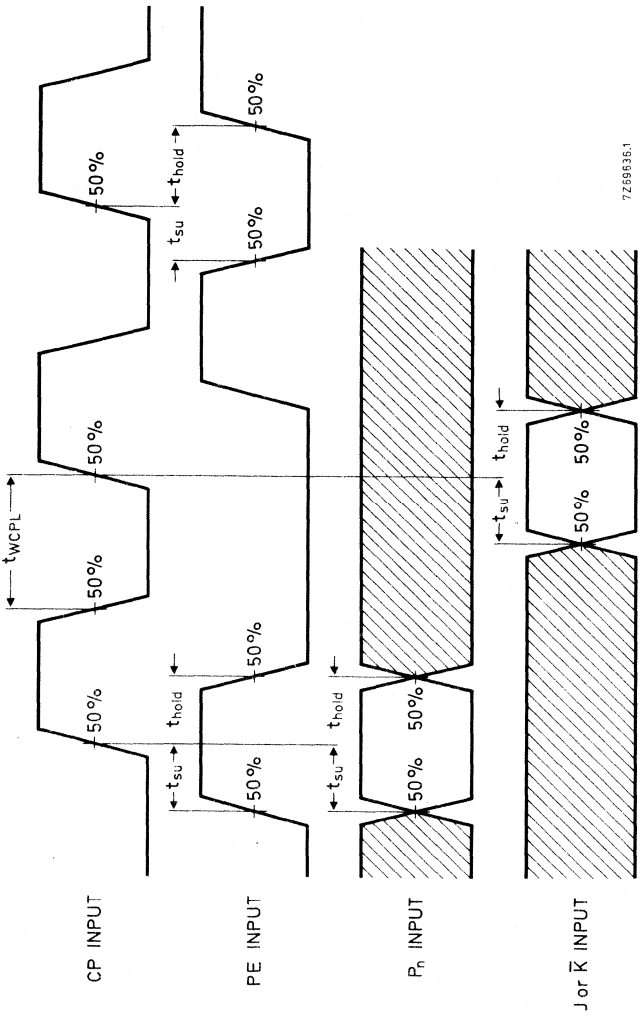
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
MR → O_n	5			175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			160	315	ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
T/$\overline{C}$ → O_n	5			115	235	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

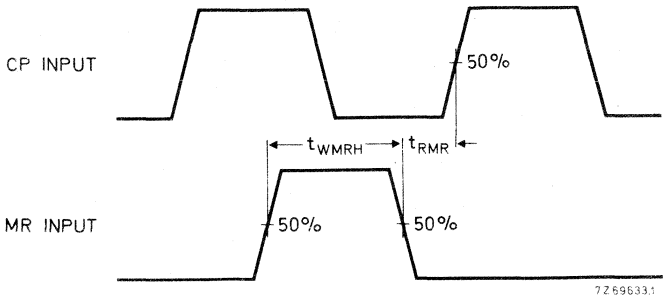
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	90	45		ns	see also waveforms on pages 6 and 7
	10		35	20		ns	
	15		25	15		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	65	30		ns	
	10		30	15		ns	
	15		20	10		ns	
Recovery time for MR	5	t_{RMR}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
Set-up times $P_n \longrightarrow CP$	5	t_{su}	215	105		ns	
	10		80	40		ns	
	15		50	25		ns	
$PE \longrightarrow CP$	5	t_{su}	200	100		ns	
	10		80	40		ns	
	15		55	25		ns	
$J, \overline{K} \longrightarrow CP$	5	t_{su}	210	105		ns	
	10		80	40		ns	
	15		50	25		ns	
Hold times $P_n \longrightarrow CP$	5	t_{hold}	35	−75		ns	
	10		10	−30		ns	
	15		5	−20		ns	
$PE \longrightarrow CP$	5	t_{hold}	10	−90		ns	
	10		5	−35		ns	
	15		5	−25		ns	
$J, \overline{K} \longrightarrow CP$	5	t_{hold}	25	−80		ns	
	10		10	−30		ns	
	15		5	−20		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		18	35		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



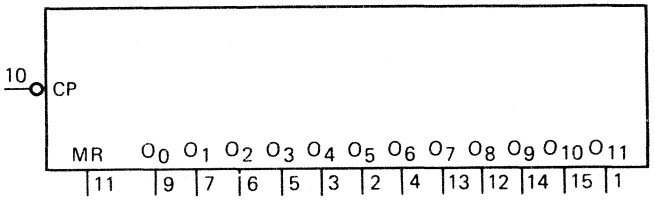
Waveforms showing minimum clock pulse width, set-up times, hold times. Set-up times and hold times are shown as positive values but may be specified as negative values.

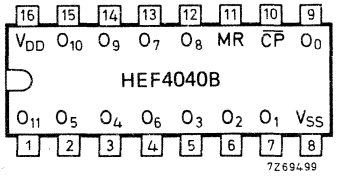


Waveforms showing minimum MR pulse width and MR recovery time.

12-STAGE BINARY COUNTER

The HEF4040B is a 12-stage binary ripple counter with a clock input ($\overline{CP}$), an overriding asynchronous master reset input (MR) and twelve fully buffered outputs (O_0 to O_{11}). The counter advances on the HIGH to LOW transition of $\overline{CP}$. A HIGH on MR clears all counter stages and forces all outputs LOW, independent of $\overline{CP}$.





HEF4040BP: 16-lead DIL; plastic (SOT-38Z).
HEF4040BD: 16-lead DIL; ceramic (SOT-74).

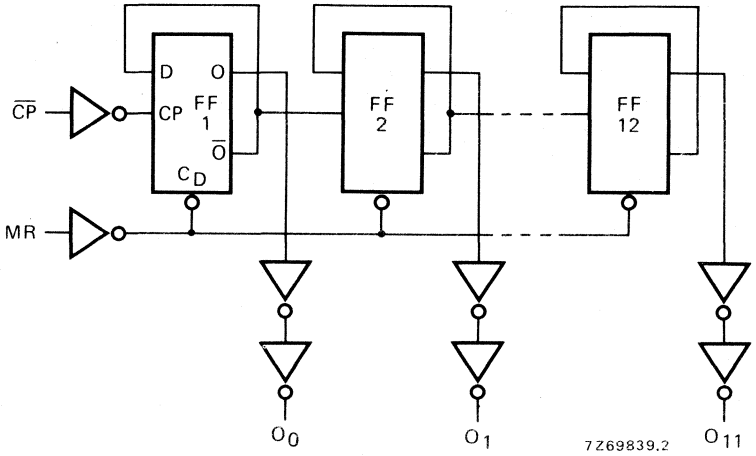
PINNING

$\overline{CP}$	clock input (HIGH to LOW edge-triggered)
MR	master reset input (active HIGH)
O_0 to O_{11}	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

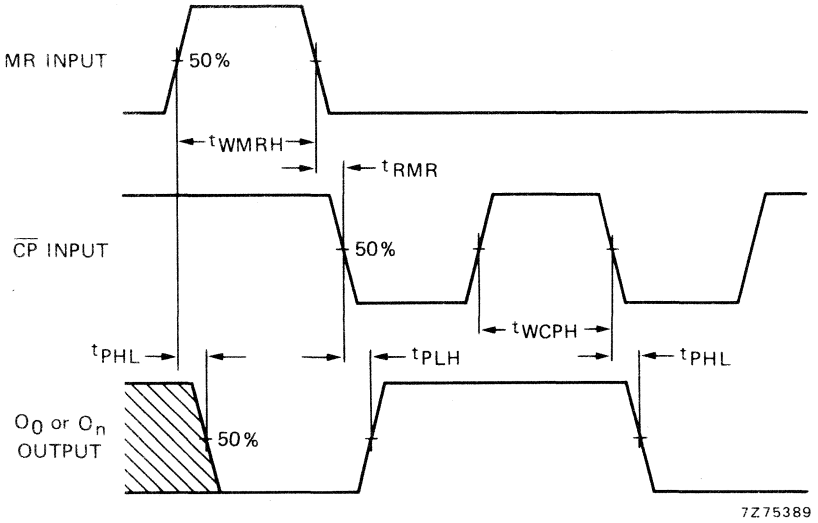
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{CP}$ → O_0	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
MR → O_n	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		90	180	ns	79 ns + (0,23 ns/pF) C_L
	15			70	140	ns	62 ns + (0,16 ns/pF) C_L
Minimum clock	5		50	25		ns	
pulse width; HIGH	10	t_{WCPH}	25	15		ns	
	15		20	10		ns	
Minimum MR	5		130	65		ns	
pulse width; HIGH	10	t_{WMRH}	95	50		ns	
	15		90	45		ns	
Recovery time	5		115	60		ns	
for MR	10	t_{RMR}	65	35		ns	
	15		55	25		ns	
Maximum clock	5		5	10		MHz	
pulse frequency	10	f_{max}	13	25		MHz	
	15		18	35		MHz	

see also waveforms on page 3

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

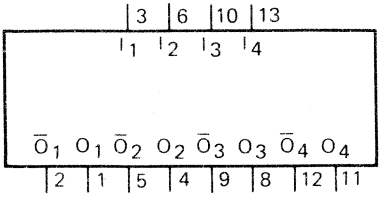
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing propagation delays for MR to O_n and $\overline{CP}$ to O_0, minimum MR and $\overline{CP}$ pulse widths.

QUADRUPLE TRUE/COMPLEMENT BUFFER

The HEF4041B is a quadruple true/complement buffer which provides both an inverted active LOW output ($\overline{O}$) and a non-inverted active HIGH output (O) for each input (I).



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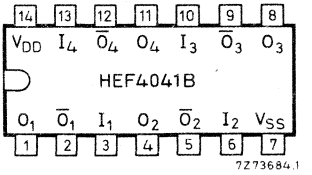
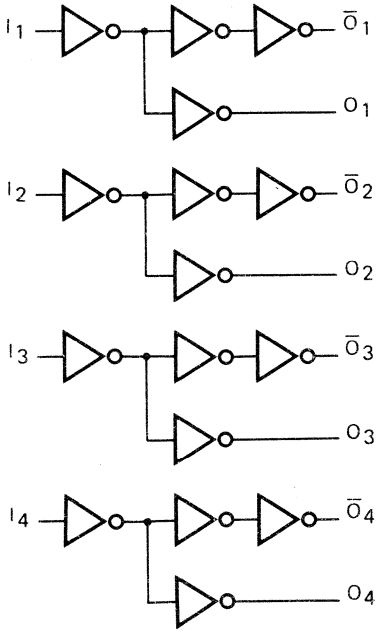


7Z73684.1

HEF4041BP : 14-lead DIL; plastic (SOT-27).
HEF4041BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



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FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 typ	+85 min	+85 max	
Output current HIGH	5	4,6		$-I_{OH}$	1,6		1,3	2,6	1,0		mA
	10	9,5			4,5		3,6	7,0	2,7		mA
	15	13,5			16,0		14,0	30,0	10,0		mA
HIGH	5	2,5		$-I_{OH}$	5,0		4,0	8,0	3,0		mA
Output current LOW	4,75		0,4		2,0		1,7	4,0	1,35		mA
	10		0,5	I_{OL}	7,5		6,0	12,0	4,5		mA
	15		1,5		23,0		20,0	35,0	15,0		mA

A.C. CHARACTERISTICS

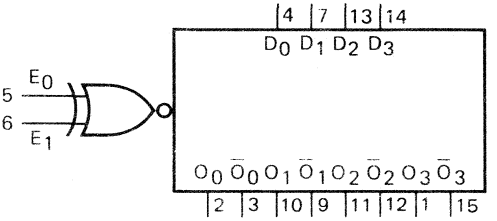
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$I_n \rightarrow O_n$	5			30	65	ns	17 ns + (0,27 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
	5			30	55	ns	17 ns + (0,27 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		15	30	ns	9 ns + (0,11 ns/pF) C_L
	15			10	20	ns	7 ns + (0,08 ns/pF) C_L
$I_n \rightarrow \overline{O}_n$	5			35	75	ns	22 ns + (0,27 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
	5			35	75	ns	22 ns + (0,27 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		20	40	ns	14 ns + (0,11 ns/pF) C_L
	15			15	30	ns	12 ns + (0,08 ns/pF) C_L
Transition times							
$O_n \rightarrow \overline{O}_n$	5			25	50	ns	5 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		12	25	ns	2 ns + (0,21 ns/pF) C_L
	15			8	20	ns	1 ns + (0,14 ns/pF) C_L
	5			25	45	ns	5 ns + (0,40 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		12	25	ns	2 ns + (0,21 ns/pF) C_L
	15			8	20	ns	1 ns + (0,14 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$12\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$33\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE D-LATCH

The HEF4042B is a 4-bit latch with four data inputs (D_0 to D_3), four buffered latch outputs (O_0 to O_3), four buffered complementary latch outputs ($\overline{O}_0$ to $\overline{O}_3$) and two common enable inputs (E_0 and E_1). Information on D_0 to D_3 is transferred to O_0 to O_3 while both E_0 and E_1 are in the same state, either HIGH or LOW. O_0 to O_3 follow D_0 to D_3 as long as both E_0 and E_1 remain in the same state. When E_0 and E_1 are different, D_0 to D_3 do not affect O_0 to O_3 and the information in the latch is stored.
$\overline{O}_0$ to $\overline{O}_3$ are always the complement of O_0 to O_3. The exclusive-OR input structure allows the choice of either polarity for E_0 and E_1. With one enable input HIGH, the other enable input is active HIGH; with one enable input LOW, the other enable input is active LOW.



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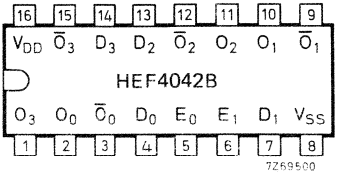


7Z69500

HEF4042BP : 16-lead DIL; plastic (SOT-38Z).
HEF4042BD: 16-lead DIL; ceramic (SOT-74).

PINNING

D_0 to D_3	data inputs
E_0 and E_1	enable inputs
O_0 to O_3	parallel latch outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary parallel latch outputs

FAMILY DATA

I_{DD} LIMITS category MSI

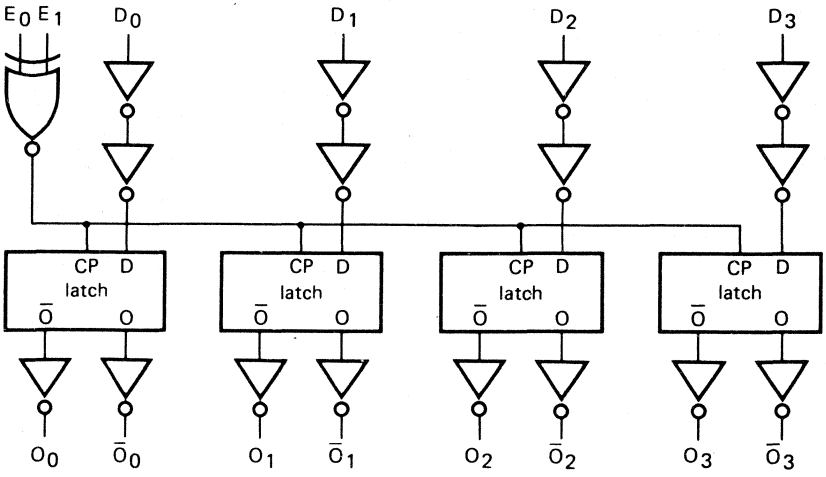
see Family Specifications

TRUTH TABLE

E_0	E_1	latch condition
L	L	enabled
L	H	not enabled
H	L	not enabled
H	H	enabled

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

LOGIC DIAGRAM



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A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

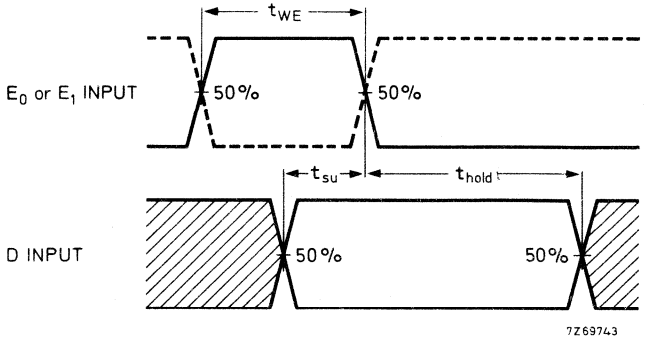
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
D ⟶ O, Ō	5			95	190	ns	67 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	28 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
	5			85	175	ns	57 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	75	ns	28 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
E ⟶ O, Ō	5			130	260	ns	102 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	105	ns	38 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			120	245	ns	92 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	38 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

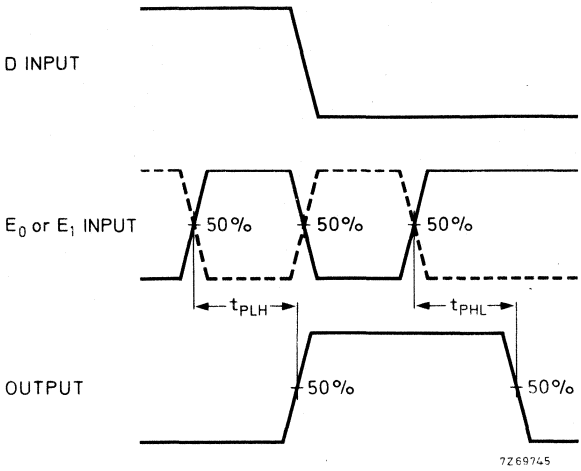
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

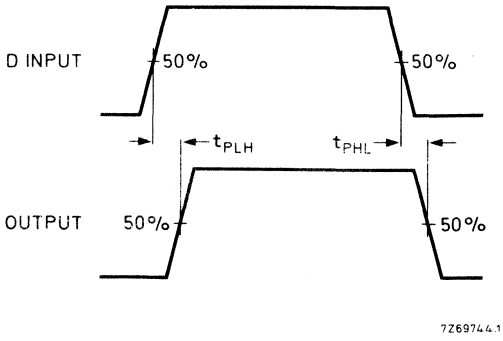
	V_{DD} V	symbol	min	typ	max		
Set-up time D → E	5	t_{su}	30	10		ns	see also waveforms below and on page 5
	10		20	5		ns	
	15		20	5		ns	
Hold time D → E	5	t_{hold}	15	−5		ns	
	10		15	0		ns	
	15		15	0		ns	
Minimum enable pulse width	5	t_{WE}	90	45		ns	
	10		40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (W)	where
Dynamic power dissipation per package (P)	5	$3800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$41\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing minimum enable pulse width, set-up time and hold time for E and D.
Set-up and hold times are shown as positive values but may be specified as negative values.





Waveforms showing propagation delays for D to O, with latch enabled.

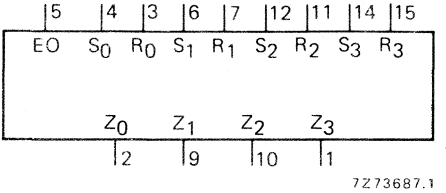
Note

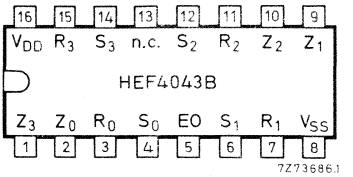
Either E_0 or E_1 is held HIGH or LOW while the other enable input is pulsed as the truth table shows (see page 1).

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS

The HEF4043B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active HIGH set input (S_0 to S_3), an active HIGH reset input (R_0 to R_3) and an active HIGH 3-state output (Z_0 to Z_3).

When EO is HIGH, the state of the latch output (Z_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.





HEF4043BP: 16-lead DIL; plastic (SOT-38Z).
HEF4043BD: 16-lead DIL; ceramic (SOT-74).

PINNING

EO	common output enable input
S_0 to S_3	set inputs (active HIGH)
R_0 to R_3	reset inputs (active HIGH)
Z_0 to Z_3	3-state buffered latch outputs

FUNCTION TABLE

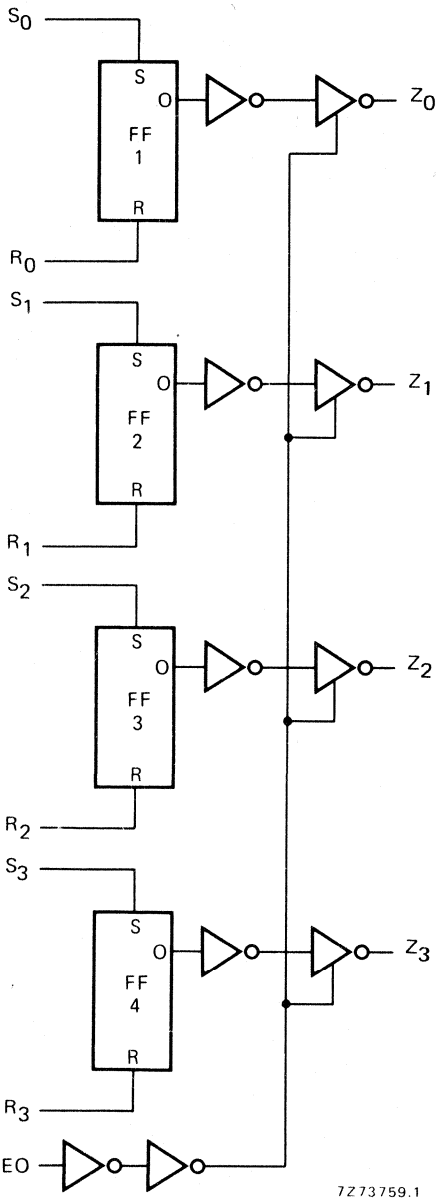
inputs			output (Z_n)
EO	S_n	R_n	
L	X	X	high impedance
H	H	L	H
H	L	H	L
H	H	H	H
H	L	L	no change

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state immaterial

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM

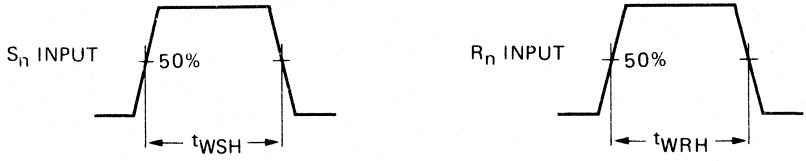


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$R_n \rightarrow Z_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$S_n \rightarrow Z_n$	5			65	135	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50	ns	14 ns + (0,23 ns/pF) C_L
	15			15	35	ns	7 ns + (0,16 ns/pF) C_L
Output disable times							
$EO \rightarrow Z_n$	5			45	90	ns	
HIGH	10	t_{PHZ}		20	35	ns	
	15			10	25	ns	
	5			50	100	ns	
LOW	10	t_{PLZ}		20	40	ns	
	15			10	25	ns	
Output enable times							
$EO \rightarrow Z_n$	5			25	50	ns	
HIGH	10	t_{PZH}		15	30	ns	
	15			10	25	ns	
	5			40	80	ns	
LOW	10	t_{PZL}		20	45	ns	
	15			15	35	ns	
Minimum S_n	5		30	15		ns	
pulse width; HIGH	10	t_{WSH}	20	10		ns	
	15		16	8		ns	
Minimum R_n	5		30	15		ns	
pulse width; HIGH	10	t_{WRH}	20	10		ns	
	15		16	8		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	11 400 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

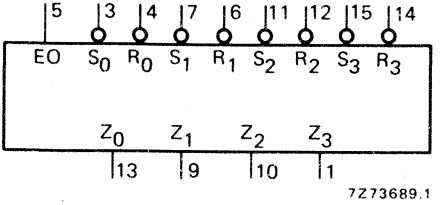


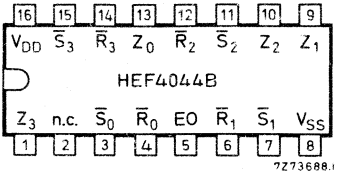
Waveforms showing minimum S_n and R_n pulse widths.

QUADRUPLE R/S LATCH WITH 3-STATE OUTPUTS

The HEF4044B is a quadruple R/S latch with 3-state outputs with a common output enable input (EO). Each latch has an active LOW set input ($\overline{S}_0$ to $\overline{S}_3$), an active LOW reset input ($\overline{R}_0$ to $\overline{R}_3$) and an active HIGH 3-state output (Z_0 to Z_3).

When EO is HIGH, the state of the latch output (Z_n) can be determined from the function table below. When EO is LOW, the latch outputs are in the high impedance OFF-state. EO does not affect the state of the latch.





HEF4044BP: 16-lead DIL; plastic (SOT-38Z).
HEF4044BD: 16-lead DIL; ceramic (SOT-74).

PINNING

EO	common output enable input
$\overline{S}_0$ to $\overline{S}_3$	set inputs (active LOW)
$\overline{R}_0$ to $\overline{R}_3$	reset inputs (active LOW)
Z_0 to Z_3	3-state buffered latch outputs

FUNCTION TABLE

inputs			output (Z_n)
EO	$\overline{S}_n$	$\overline{R}_n$	
L	X	X	high impedance
H	L	H	H
H	H	L	L
H	L	L	L
H	H	H	no change

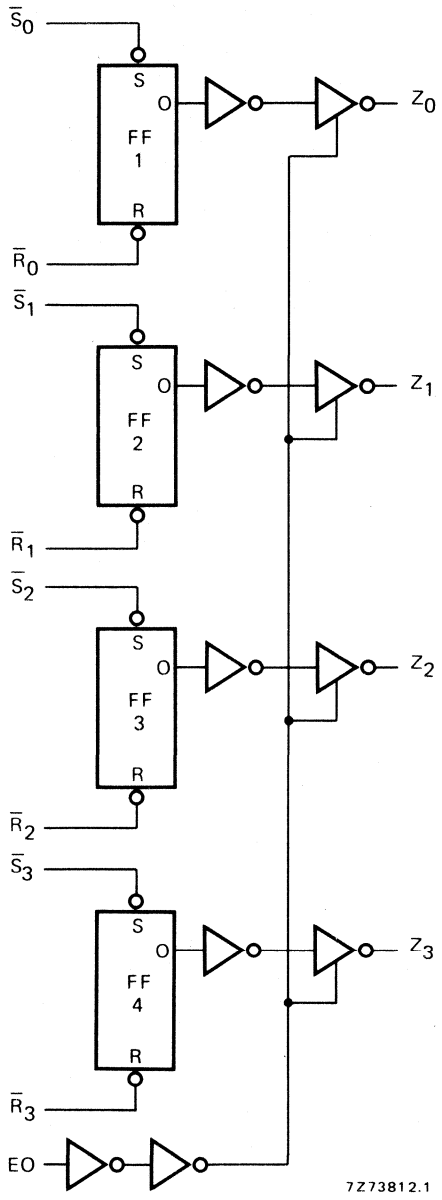
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

LOGIC DIAGRAM

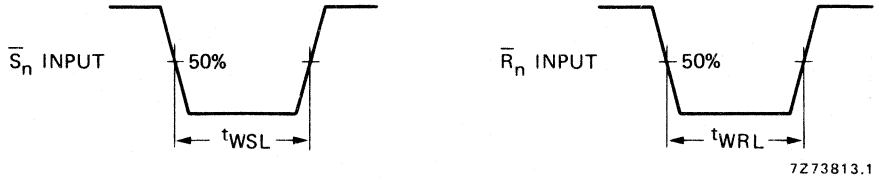


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{R}_n \rightarrow Z_n$	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{S}_n \rightarrow Z_n$	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Output disable times							
EO $\rightarrow Z_n$	5			50	100	ns	
HIGH	10	t_{PHZ}		30	60	ns	
	15			25	50	ns	
	5			30	60	ns	
LOW	10	t_{PLZ}		25	45	ns	
	15			20	40	ns	
Output enable times							
EO $\rightarrow Z_n$	5			50	100	ns	
HIGH	10	t_{PZH}		25	50	ns	
	15			20	40	ns	
	5			50	95	ns	
LOW	10	t_{PZL}		25	45	ns	
	15			20	35	ns	
Minimum $\overline{S}_n$	5		30	15		ns	
pulse width; LOW	10	t_{WSL}	20	10		ns	
	15		16	8		ns	
Minimum $\overline{R}_n$	5		30	15		ns	
pulse width; LOW	10	t_{WRL}	20	10		ns	
	15		16	8		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1300 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	5200 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	12 900 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	



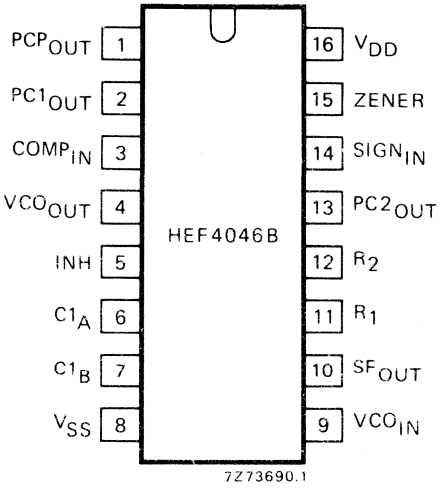
Waveforms showing minimum $\overline{S}_n$ and $\overline{R}_n$ pulse widths.

PHASE-LOCKED LOOP

The HEF4046B phase-locked loop circuit contains two phase comparators, a voltage controlled oscillator (VCO), source-followers and a zener diode. The comparators have two common inputs, $COMP_{IN}$ and $SIGN_{IN}$. $SIGN_{IN}$ can be directly coupled to large voltage signals or indirectly coupled (with a series capacitor) to small voltage signals. The self-biasing circuit adjusts small voltage signals in the linear region of the amplifier.

Phase comparator 1 (an EXCLUSIVE-OR gate) provides a digital error signal at $PC1_{OUT}$ and maintains 90^{o} phase shift at the centre frequency between the $SIGN_{IN}$ and $COMP_{IN}$ signals (both at 50% duty factor). Phase comparator 2 (with leading-edge sensing logic) provides digital error signals at $PC2_{OUT}$ and PCP_{OUT}, and maintains a 0^{o} phase shift between the $SIGN_{IN}$ and $COMP_{IN}$ signals (duty factor is immaterial). The linear VCO produces an output signal at VCO_{OUT} whose frequency is determined by the voltage of VCO_{IN} and the capacitor and resistors connected to pins $C1_A$, $C1_B$, R_1 and R_2. The source-follower output (SF_{OUT}) with an external resistor is used when the VCO_{IN} signal is needed, but no loading can be tolerated. The inhibit input (INH), when HIGH, disables the VCO and source follower to minimize stand-by power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

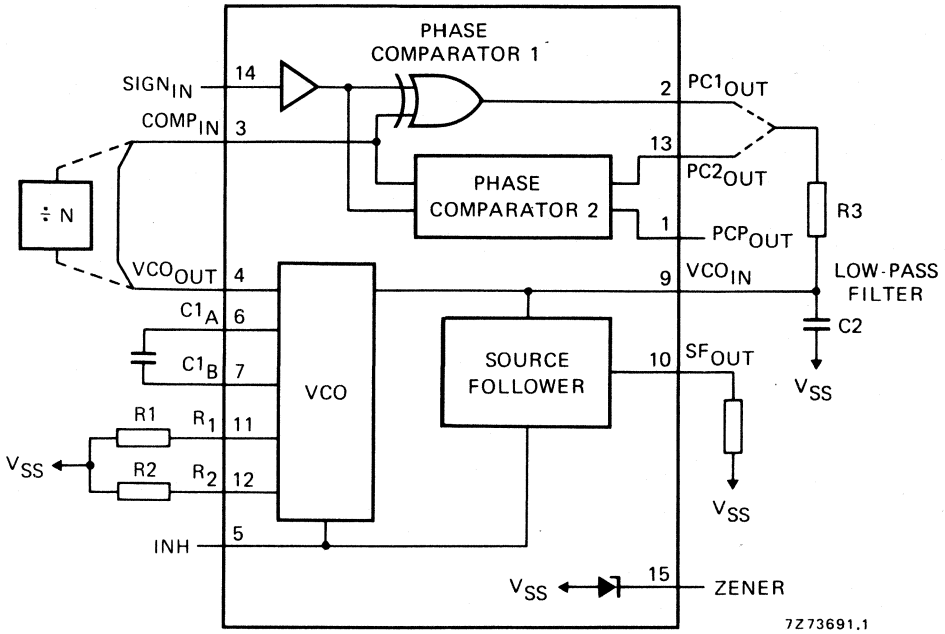


HEF4046BP: 16-lead DIL; plastic (SOT-38Z).
HEF4046BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA: see Family Specifications.

I_{DD} LIMITS category MSI: see page 2.

BLOCK DIAGRAM



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 typ	+ 25 typ	+ 85 typ	
Quiescent device current	5	I_{DD} *		20		μA
	10			200		μA
	15			700		μA
Quiescent device current	5	I_{DD} **		10		μA
	10			40		μA
	15			80		μA

* Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.
** Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD} or V_{SS}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Phase comparators							
Operating supply voltage		V_{DD}	3		15	V	comparators only
			5		15	V	VCO operation
Input resistance at $SIGN_{IN}$	5	R_{IN}		600		kΩ	see note 1
	10			200		kΩ	
	15			100		kΩ	
A.C. coupled input sensitivity at $SIGN_{IN}$	5	V_{IN}		200		mV	
	10			400		mV	
	15			700		mV	
VCO							
Operating supply voltage		V_{DD}	3		15	V	as fixed oscillator only
			5		15	V	phase-locked loop operation
Maximum operating frequency	5	f_{max}		0,5		MHz	see note 2
	10			1,2		MHz	see note 3
	15			1,5		MHz	
Output duty factor	5	δ		50		%	
	10			50		%	
	15			50		%	
Zener diode							
Zener voltage	5	V_Z		7,5		V	I_Z = 50 μA
	10			7,5		V	
	15			7,5		V	
Dynamic resistance	5	R_Z		100		Ω	I_Z = 1 mA
	10			100		Ω	
	15			100		Ω	

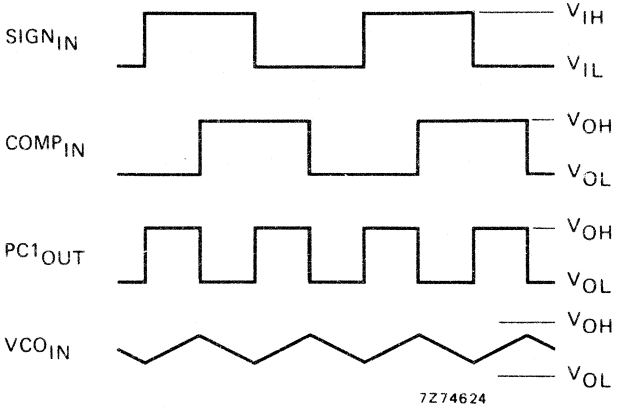
NOTES

1. D.C. level of $SIGN_{IN}$ voltage is ½ V_{DD}.
2. R1 = 10 kΩ; R2 = ∞; VCO_{IN} at V_{DD}; C1 = 100 pF.
3. R1 = 10 kΩ; R2 = ∞; VCO_{IN} at V_{DD}; C1 = 50 pF.

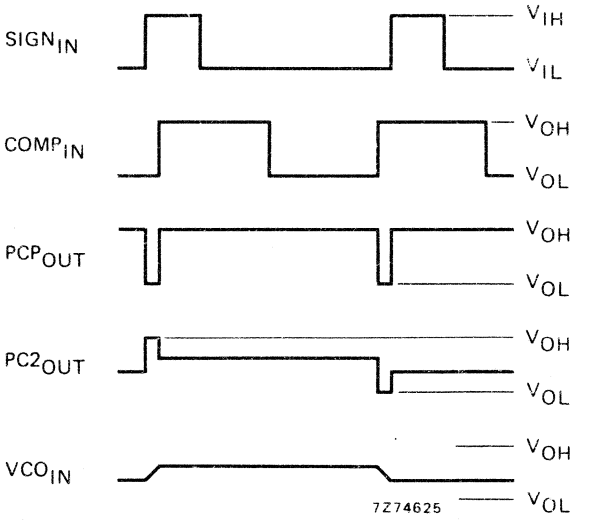
DEVELOPMENT SAMPLE DATA

DESIGN INFORMATION

characteristic	using phase comparator 1	using phase comparator 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90^o at centre frequency (f_o), approching 0^o and 180^o at ends of lock range ($2\ f_L$)	always 0^o in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range ($2\ f_L$)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; $2\ f_L$ = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range ($2\ f_C$)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics	$f_C = f_L$



Typical waveforms for phase-locked loop employing phase comparator 1 in locked condition of f_o.

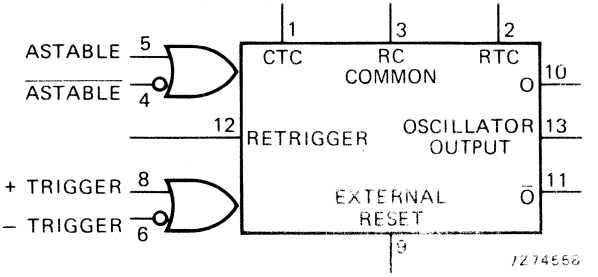


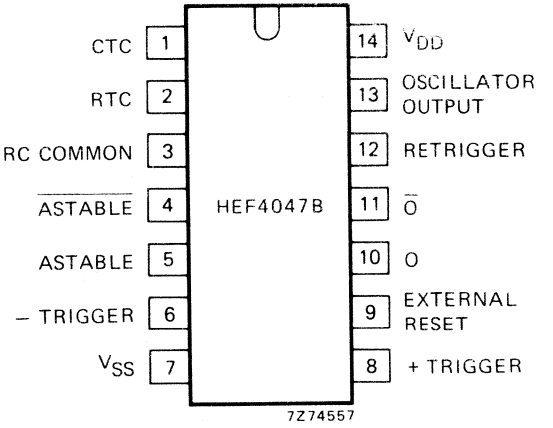
Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

MONOSTABLE/ASTABLE MULTIVIBRATOR

The HEF4047B consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include + TRIGGER, – TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER and EXTERNAL RESET. Buffered outputs are O, $\overline{O}$ and OSCILLATOR OUTPUT. In all modes of operation an external capacitor must be connected between C-timing (CTC) and RC COMMON, and an external resistor must be connected between R-timing (RTC) and RC COMMON (continued on page 2).





HEF4047BP: 14-lead DIL; plastic (SOT-27).
HEF4047BD: 14-lead DIL; ceramic (SOT-73).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

Astable operation is enabled by a HIGH level on the ASTABLE input. The period of the square wave at O and $\overline{O}$ outputs is a function of the external components employed. 'True' input pulses on the ASTABLE or 'complement' pulses on the $\overline{\text{ASTABLE}}$ input, allow the circuit to be used as a gatable multivibrator. The OSCILLATOR OUTPUT period will be half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the + TRIGGER input and a LOW level to the −TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the −TRIGGER and a HIGH level to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option can be implemented by coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator. A HIGH level on the EXTERNAL RESET input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to the EXTERNAL RESET, whenever V_{DD} is applied.

FUNCTIONAL CONNECTIONS

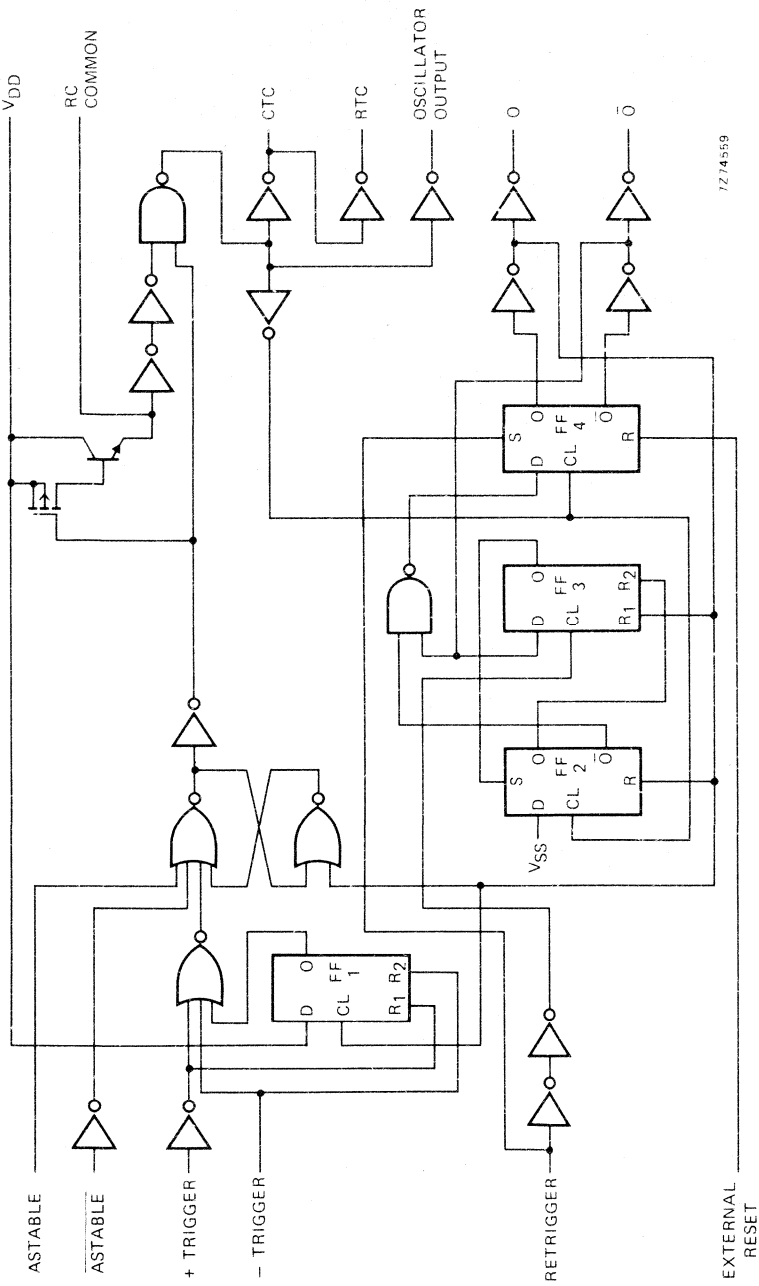
function	pins connected to			output pulse from pins
	V_{DD}	V_{SS}	input pulse	
astable multivibrator				
free running	4, 5, 6, 14	7, 8, 9, 12	–	10, 11, 13
true gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13
complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13
monostable multivibrator				
pos. edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11
neg. edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11
retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11
external count down	14	5, 6, 7, 8, 9, 12	–	10, 11

Note

In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

DEVELOPMENT SAMPLE DATA

LOGIC DIAGRAM



D.C. CHARACTERISTICS

V_{SS} = 0 V; inputs at 0 V or V_{DD}

	V_{DD} V	$-I_{OH}$ mA	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output voltage HIGH; pin 3	5	5	V_{OH}	2,0		2,0		1,7		V
	10	10		5,5		5,5		5,2		V
	15	14		9,3		9,3		9,0		V

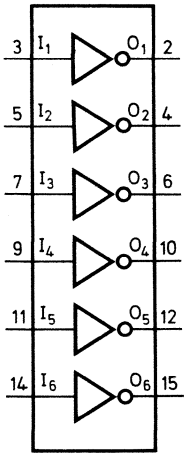
A.C. CHARACTERISTICS

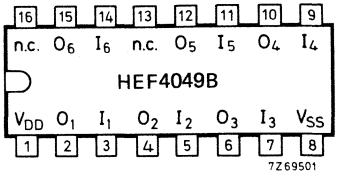
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Propagation delays						
ASTABLE, $\overline{\text{ASTABLE}}$ → OSC. OUTPUT						
HIGH to LOW;	5	t_{PHL};		120		ns
LOW to HIGH	10	t_{PLH}		60		ns
	15			–		ns
ASTABLE, $\overline{\text{ASTABLE}}$ → O, $\overline{\text{O}}$						
HIGH to LOW;	5	t_{PHL};		330		ns
LOW to HIGH	10	t_{PLH}		150		ns
	15			–		ns
+/−TRIGGER → O, $\overline{\text{O}}$						
HIGH to LOW;	5	t_{PHL};		420		ns
LOW to HIGH	10	t_{PLH}		180		ns
	15			–		ns
+TRIGGER, RETRIGGER → O, $\overline{\text{O}}$						
HIGH to LOW;	5	t_{PHL};		180		ns
LOW to HIGH	10	t_{PLH}		105		ns
	15			–		ns
EXTERNAL RESET → O, $\overline{\text{O}}$						
HIGH to LOW;	5	t_{PHL};		180		ns
LOW to HIGH	10	t_{PLH}		75		ns
	15			–		ns
Transition times						
HIGH to LOW;	5	t_{THL};		45		ns
LOW to HIGH	10	t_{TLH}		25		ns
	15			–		ns
Minimum input pulse width;	5			300		ns
any input	10	t_W		120		ns
	15			–		ns

HEX INVERTING BUFFERS

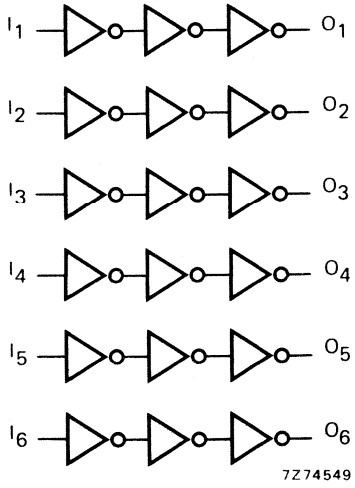
The HEF4049B provides six inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table on page 2.





HEF4049BP : 16-lead DIL; plastic (SOT-38Z).
HEF4049BD: 16-lead DIL; ceramic (SOT-74).

LOGIC DIAGRAM



FAMILY DATA

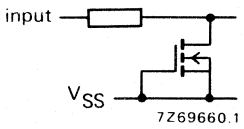
I_{DD} LIMITS category BUFFERS

see Family Specifications

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current LOW	4,75	0,4	I_{OL}	3,5		2,9		2,3		mA
	10	0,5		12,0		10,0		8,0		mA
	15	1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

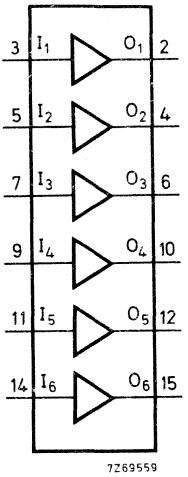
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	50	100	ns	41 ns + (0,18 ns/pF) C_L
	10		20	45	ns	16 ns + (0,08 ns/pF) C_L
	15		15	30	ns	13 ns + (0,05 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	60	125	ns	33 ns + (0,55 ns/pF) C_L
	10		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
Transition time HIGH to LOW	5	t_{THL}	25	50	ns	7 ns + (0,35 ns/pF) C_L
	10		10	20	ns	3 ns + (0,14 ns/pF) C_L
	15		7	14	ns	2 ns + (0,09 ns/pF) C_L

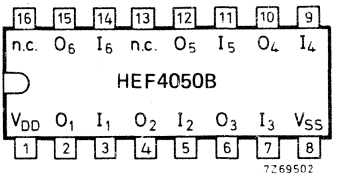
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$15\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$55\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

HEX NON-INVERTING BUFFERS

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in the table on page 2.



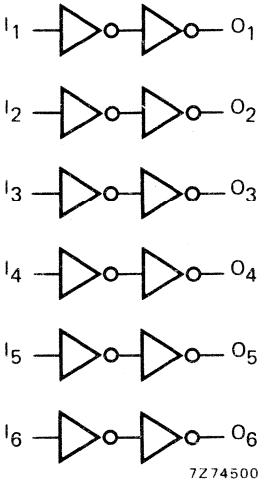
7Z69559



7Z69502

HEF4050BP: 16-lead DIL; plastic (SOT-38Z).
HEF4050BD: 16-lead DIL; ceramic (SOT-74).

LOGIC DIAGRAM



7Z74500

FAMILY DATA

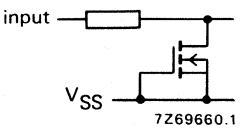
I_{DD} LIMITS catagory BUFFERS

} see Family Specifications

Guaranteed fan-out in common logic families

driven element	guaranteed fan-out
standard TTL	2
74LS	9
74L	16

Input protection



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current LOW	4,75	0,4	I_{OL}	3,5		2,9		2,3		mA
	10	0,5		12,0		10,0		8,0		mA
	15	1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	35	70	ns	26 ns + (0,18 ns/pF)C_L
	10		20	35	ns	16 ns + (0,08 ns/pF)C_L
	15		15	30	ns	12 ns + (0,05 ns/pF)C_L
LOW to HIGH	5	t_{PLH}	55	110	ns	28 ns + (0,55 ns/pF)C_L
	10		25	55	ns	14 ns + (0,23 ns/pF)C_L
	15		20	40	ns	12 ns + (0,16 ns/pF)C_L
Transition time HIGH to LOW	5	t_{THL}	25	50	ns	7 ns + (0,35 ns/pF)C_L
	10		10	20	ns	3 ns + (0,14 ns/pF)C_L
	15		7	14	ns	2 ns + (0,09 ns/pF)C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$3800\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$11\,600\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$65\,900\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_oC_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

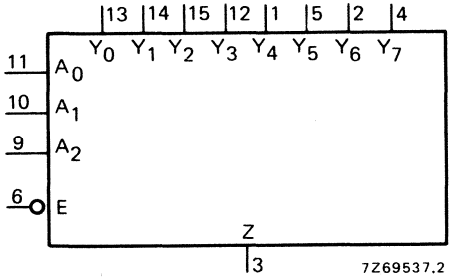
8-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

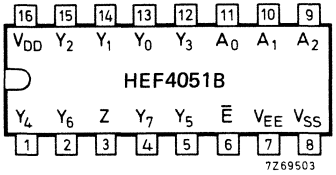
The HEF4051B is an 8-channel analogue multiplexer/demultiplexer with three address inputs (A_0 to A_2), an active LOW enable input ($\overline{E}$), eight independent inputs/outputs (Y_0 to Y_7) and a common input/output (Z).

The device contains eight bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_7) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the eight switches is selected (low impedance ON-state) by A_0 to A_2. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 to A_2.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0 to A_2, and $\overline{E}$). Their voltage limits are 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_7, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.





HEF4051BP: 16-lead DIL; plastic (SOT-38Z).
HEF4051BD: 16-lead DIL; ceramic (SOT-74).

PINNING

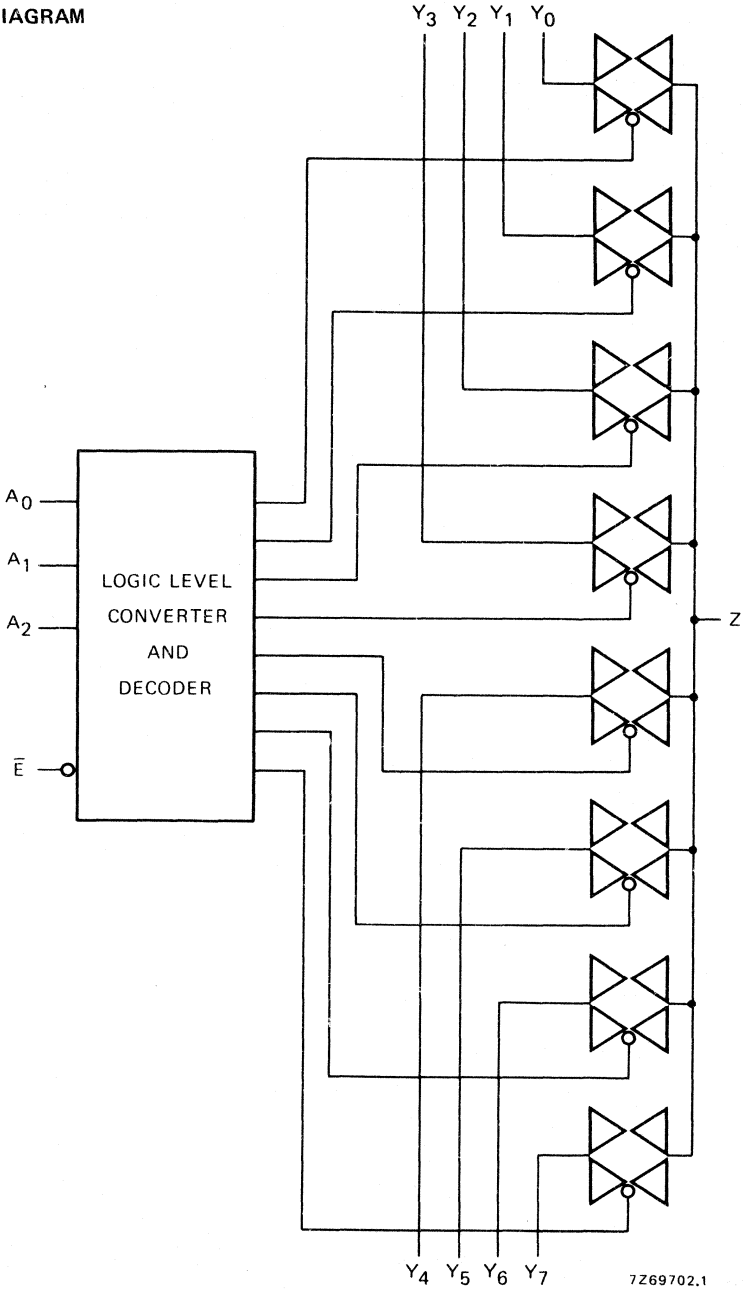
Y_0 to Y_7	independent inputs/outputs
A_0 to A_2	address inputs
$\overline{E}$	enable input (active LOW)
Z	common input/output

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs				channel ON
$\overline{E}$	A_2	A_1	A_0	
L	L	L	L	Y_0–Z
L	L	L	H	Y_1–Z
L	L	H	L	Y_2–Z
L	L	H	H	Y_3–Z
L	H	L	L	Y_4–Z
L	H	L	H	Y_5–Z
L	H	H	L	Y_6–Z
L	H	H	H	Y_7–Z
H	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	350	1050	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig. 1
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_i = 0 see Fig. 1
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	$V_i = V_{DD}-V_{EE}$ see Fig. 1
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	15	–	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig. 1
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

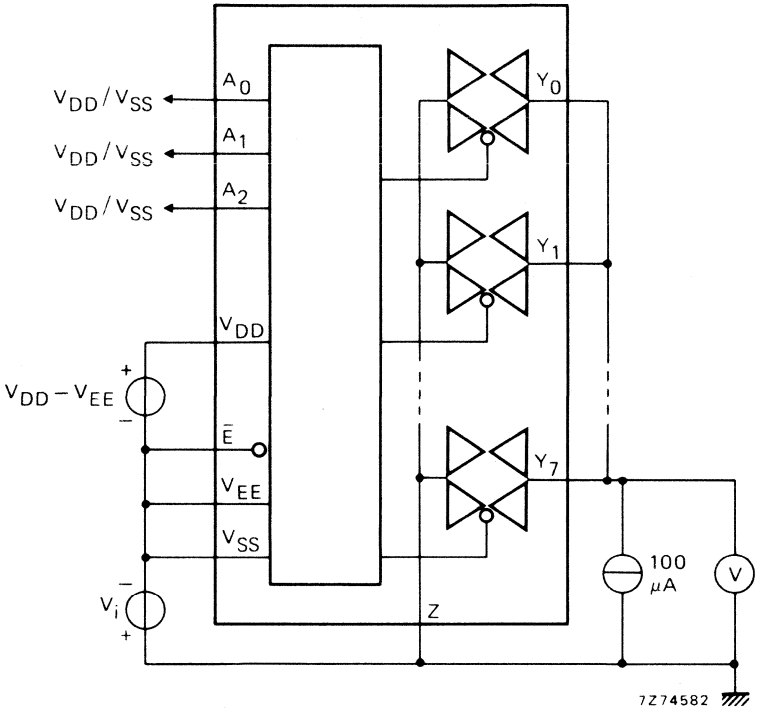


Fig. 1 Test set-up for measuring R_{ON}.

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	15	25	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
LOW to HIGH	5	t_{PLH}	15	25	ns	note 1
	10		5	10	ns	
	15		5	10	ns	
$A_n \rightarrow V_{os}$						
HIGH to LOW	5	t_{PHL}	170	345	ns	note 2
	10		65	125	ns	
	15		50	100	ns	
LOW to HIGH	5	t_{PLH}	160	320	ns	note 2
	10		65	130	ns	
	15		45	90	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PHZ}	125	250	ns	note 3
	10		90	180	ns	
	15		85	170	ns	
LOW	5	t_{PLZ}	155	310	ns	note 3
	10		120	240	ns	
	15		115	230	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$						
HIGH	5	t_{PZH}	190	380	ns	note 3
	10		75	145	ns	
	15		50	100	ns	
LOW	5	t_{PZL}	195	385	ns	note 3
	10		75	145	ns	
	15		50	100	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ	max	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; A_n is V_{DD} (square-wave); $V_{is} = V_{DD}$ or V_{EE}; see Fig. 2.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E}$ is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{EE} for t_{PHZ} and t_{PZH};
   V_{is} at V_{EE} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD}); $f_{is} = 1$ kHz; see Fig. 3.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 4.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or A_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value); see Fig. 2.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 3.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p-p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 3.

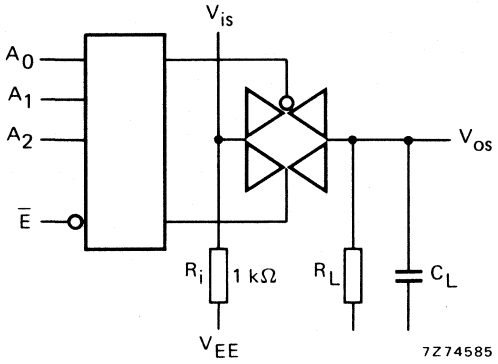


Fig. 2

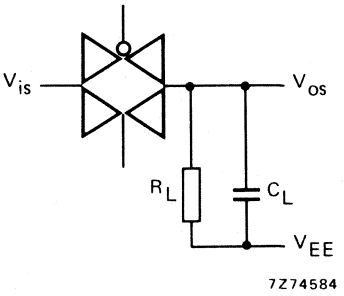
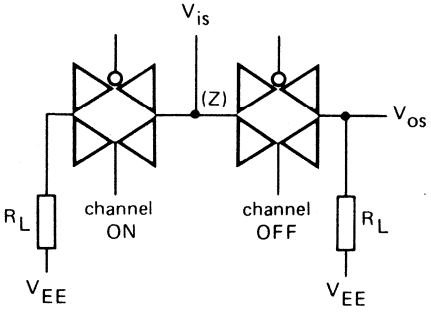
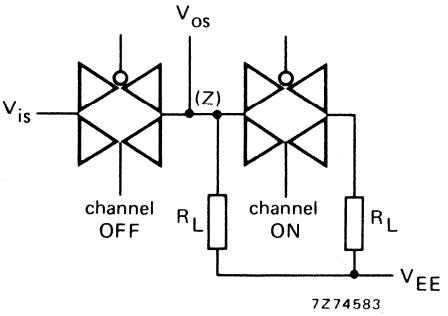


Fig. 3



(a)



(b)

Fig. 4

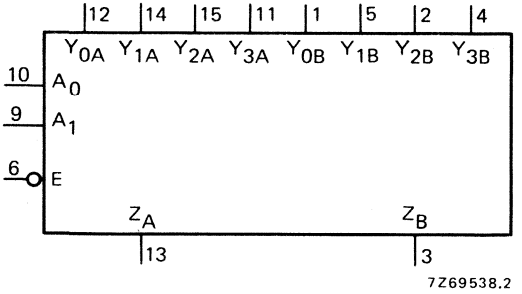
DUAL 4-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4052B is a dual 4-channel analogue multiplexer/demultiplexer with common channel select logic. Each multiplexer/demultiplexer has four independent inputs/outputs (Y_0 to Y_3) and a common input/output (Z). The common channel select logic includes two address inputs (A_0 and A_1) and an active LOW enable input ($\overline{E}$).

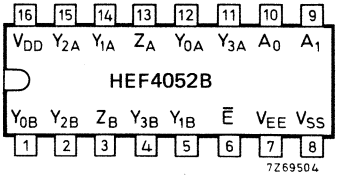
Both multiplexers/demultiplexers contain four bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_3) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the four switches is selected (low impedance ON-state) by A_0 and A_1. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of A_0 and A_1.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (A_0, A_1 and $\overline{E}$). Their voltage limits are 3 to 15 V. The analogue inputs/outputs (Y_0 to Y_3, and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.



7Z69538.2



7Z69504

HEF4052BP: 16-lead DIL; plastic (SOT-38Z).
HEF4052BD: 16-lead DIL; ceramic (SOT-74).

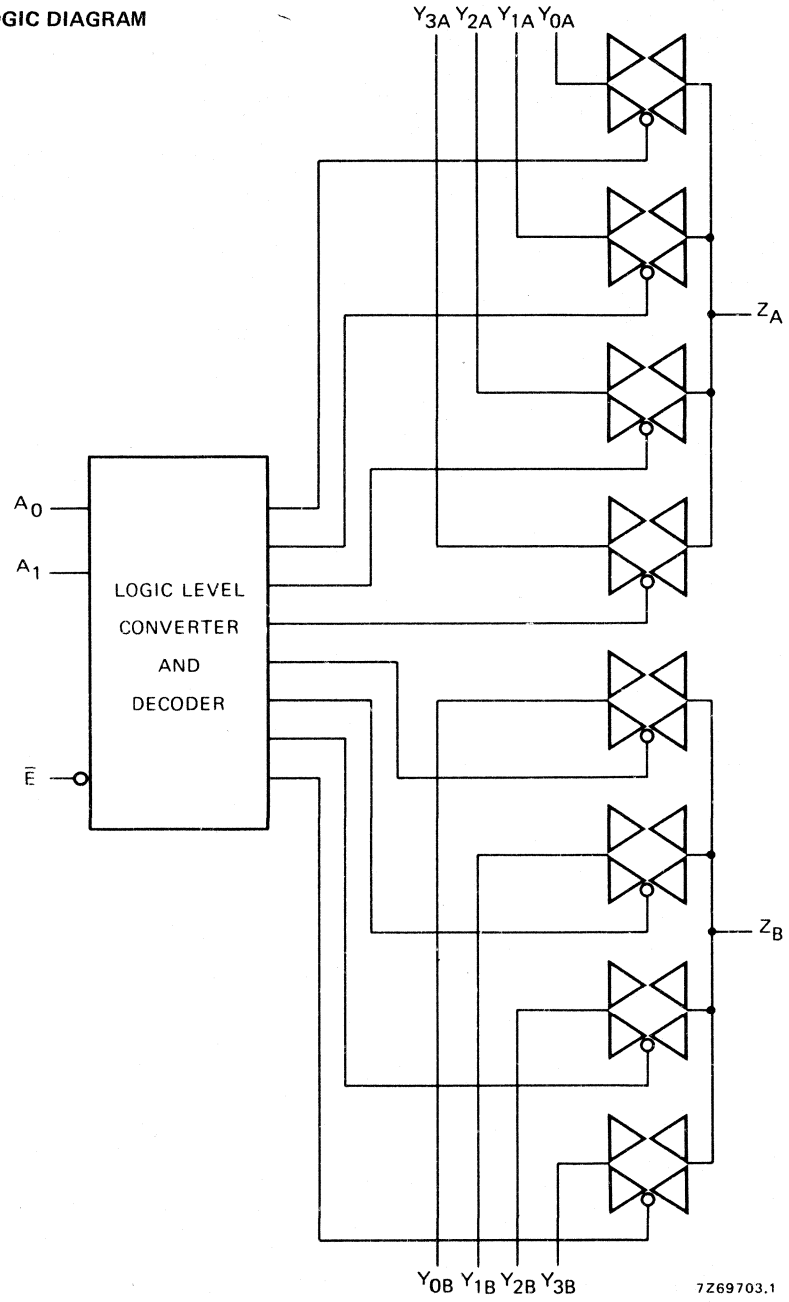
PINNING

Y_{0A} to Y_{3A}	independent inputs/outputs
Y_{0B} to Y_{3B}	independent inputs/outputs
A_0, A_1	address inputs
$\overline{E}$	enable input (active LOW)
Z_A, Z_B	common inputs/outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs			channel ON
$\overline{E}$	A_1	A_0	
L	L	L	Y_{0A}–Z_A; Y_{0B}–Z_B
L	L	H	Y_{1A}–Z_A; Y_{1B}–Z_B
L	H	L	Y_{2A}–Z_A; Y_{2B}–Z_B
L	H	H	Y_{3A}–Z_A; Y_{3B}–Z_B
H	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	350	1050	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig. 1
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_i = 0 see Fig. 1
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	$V_i = V_{DD}-V_{EE}$ see Fig. 1
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	15	–	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig.1
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

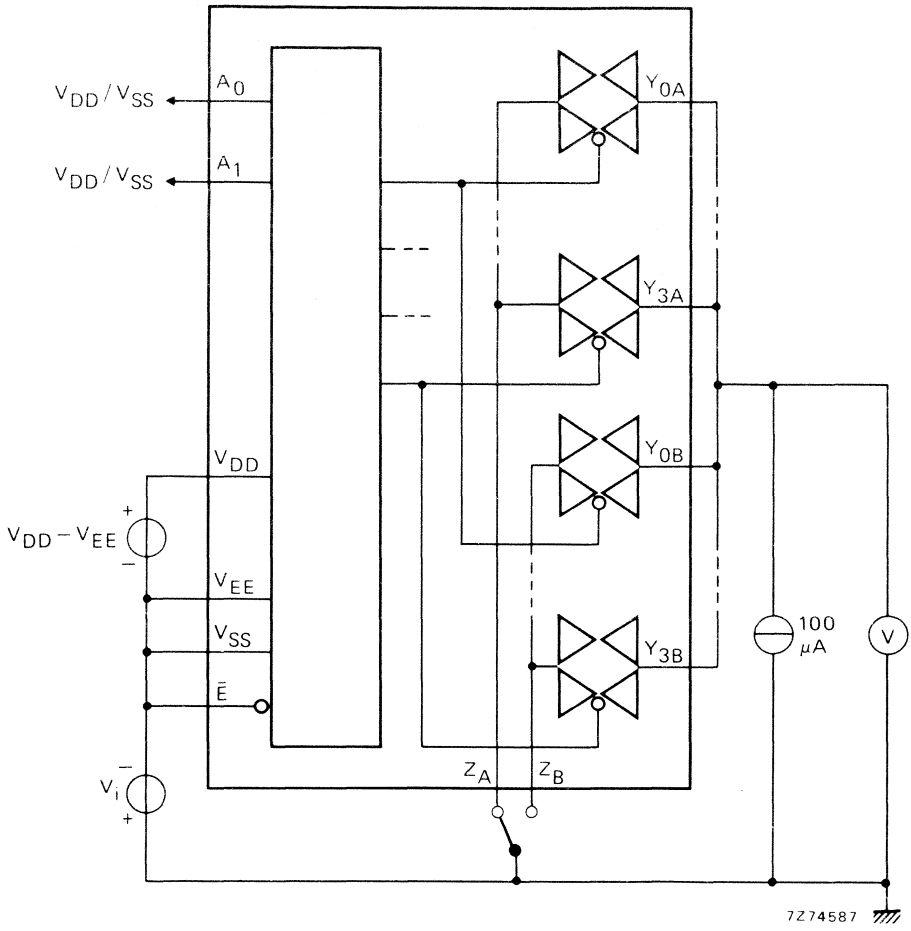


Fig. 1 Test set-up for measuring R_{ON}.

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$15\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		10	20	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
$A_n \rightarrow V_{os}$	5		150	305	ns	
HIGH to LOW	10	t_{PHL}	65	135	ns	note 2
	15		50	100	ns	
	5		75	150	ns	
LOW to HIGH	10	t_{PLH}	35	75	ns	note 2
	15		30	55	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		100	205	ns	
HIGH	10	t_{PHZ}	90	180	ns	note 3
	15		90	180	ns	
	5		95	190	ns	
LOW	10	t_{PLZ}	90	180	ns	note 3
	15		90	180	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		130	260	ns	
HIGH	10	t_{PZH}	55	115	ns	note 3
	15		45	85	ns	
	5		120	240	ns	
LOW	10	t_{PZL}	50	100	ns	note 3
	15		35	75	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times $\leqslant 20$ ns

	V_{DD} V	symbol	typ	max	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; A_n is V_{DD} (square-wave); $V_{is} = V_{DD}$ or V_{EE}; see Fig. 2.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E}$ is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{EE} for t_{PHZ} and t_{PZH};
   V_{is} at V_{EE} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = \frac{1}{2} V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$); $f_{is} = 1$ kHz; see Fig. 3.
5. $R_L = 1$ kΩ; $V_{is} = \frac{1}{2} V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 4.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or A_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value); see Fig. 2.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = \frac{1}{2} V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 3.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = \frac{1}{2} V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $\frac{1}{2} V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 3.

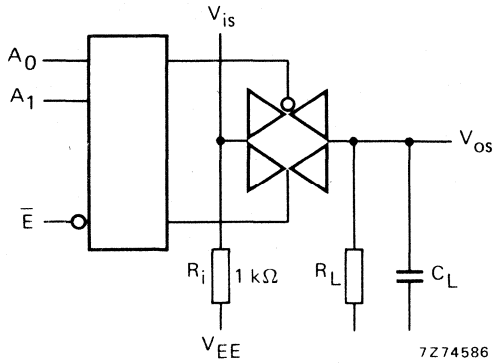


Fig. 2

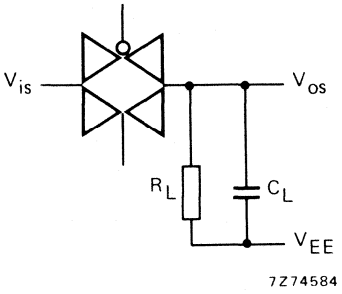
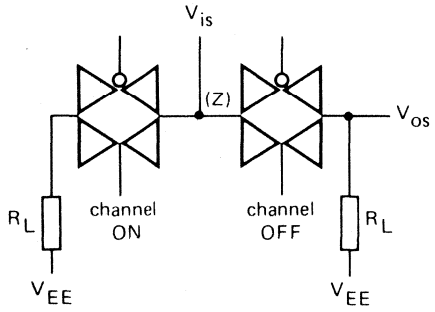
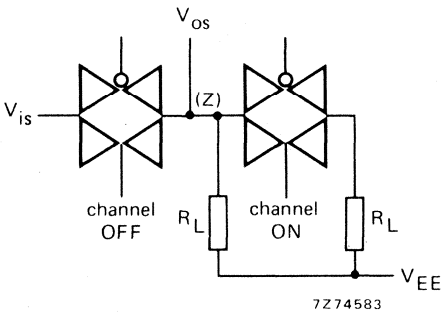


Fig. 3



(a)



(b)

Fig. 4

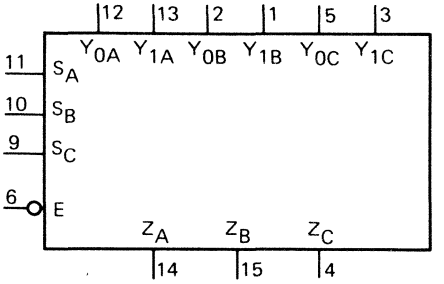
TRIPLE 2-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

The HEF4053B is a triple 2-channel analogue multiplexer/demultiplexer with a common enable input ($\overline{E}$). Each multiplexer/demultiplexer has two independent inputs/outputs (Y_0 and Y_1), a common input/output (Z), and select inputs (S_n). Each also contains two-bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 and Y_1) and the other side connected to a common input/output (Z).

With $\overline{E}$ LOW, one of the two switches is selected (low impedance ON-state) by S_n. With $\overline{E}$ HIGH, all switches are in the high impedance OFF-state, independent of S_A to S_C.

V_{DD} and V_{SS} are the supply voltage connections for the digital control inputs (S_A to S_C and $\overline{E}$). Their voltage limits are the same as for all other digital LOCMOS. The analogue inputs/outputs (Y_0, Y_1 and Z) can swing between V_{DD} as a positive limit and V_{EE} as a negative limit. $V_{DD} - V_{EE}$ may not exceed 15 V.

For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to V_{SS} (typically ground).



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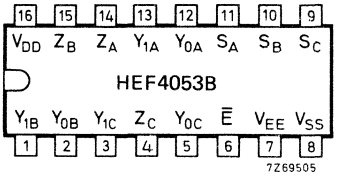


7Z69505

HEF4053BP: 16-lead DIL; plastic (SOT-38Z).
HEF4053BD: 16-lead DIL; ceramic (SOT-74).

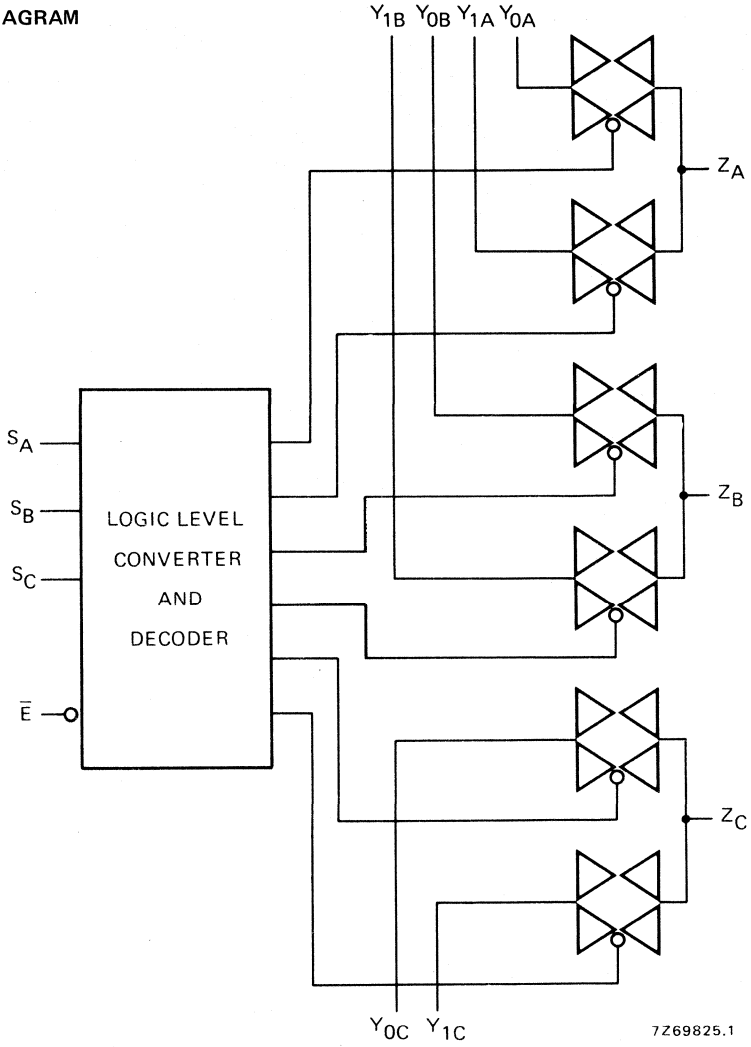
PINNING

Y_{0A} to Y_{0C}	independent inputs/outputs
Y_{1A} to Y_{1C}	independent inputs/outputs
S_A to S_C	select inputs
$\overline{E}$	enable input (active LOW)
Z_A to Z_C	common inputs/outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs		channel ON
$\overline{E}$	S_A	
L	L	Y_{0A}–Z_A
L	H	Y_{1A}–Z_A
H	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (with reference to V_{DD}) V_{EE} −18 to + 0,5 V

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	$V_{DD}-V_{EE}$ V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	350	1050	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig. 1
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_i = 0 see Fig. 1
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_i = $V_{DD}-V_{EE}$ see Fig. 1
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	15	–	Ω	V_i = 0 to $V_{DD}-V_{EE}$ see Fig. 1
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

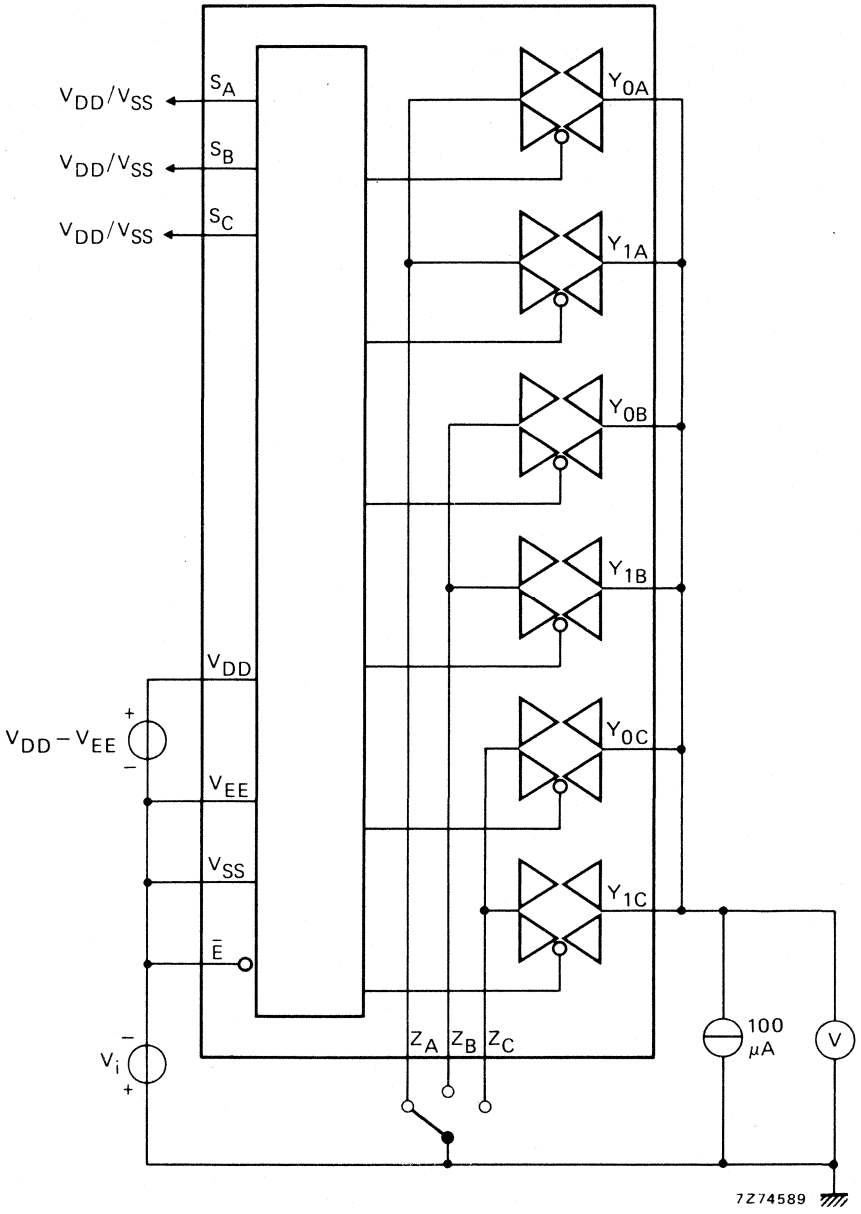


Fig. 1 Test set-up for measuring R_{ON}.

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$11\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$29\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		15	30	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
$S_n \rightarrow V_{os}$	5		200	400	ns	
HIGH to LOW	10	t_{PHL}	85	170	ns	note 2
	15		65	130	ns	
	5		275	555	ns	
LOW to HIGH	10	t_{PLH}	100	200	ns	note 2
	15		65	130	ns	
Output disable times						
$\overline{E} \rightarrow V_{os}$	5		200	400	ns	
HIGH	10	t_{PHZ}	115	230	ns	note 3
	15		110	220	ns	
	5		200	400	ns	
LOW	10	t_{PLZ}	120	245	ns	note 3
	15		110	215	ns	
Output enable times						
$\overline{E} \rightarrow V_{os}$	5		260	525	ns	
HIGH	10	t_{PZH}	95	190	ns	note 3
	15		65	130	ns	
	5		280	565	ns	
LOW	10	t_{PZL}	105	205	ns	note 3
	15		70	140	ns	

A.C. CHARACTERISTICS

$V_{EE} = V_{SS} = 0$ V; $T_{amb} = 25$ °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. $R_L = 10$ kΩ to V_{EE}; $C_L = 50$ pF to V_{EE}; $\overline{E}$ at V_{SS}; S_n is V_{DD} (square-wave); $V_{is} = V_{DD}$ or V_{EE}; see Fig. 2.
3. $R_L = 10$ kΩ; $C_L = 50$ pF to V_{EE}; $\overline{E}$ is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{EE} for t_{PHZ} and t_{PZH};
   V_{is} at V_{EE} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
4. $R_L = 10$ kΩ; $C_L = 15$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$); $f_{is} = 1$ kHz; see Fig. 3.
5. $R_L = 1$ kΩ; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 4.
6. $R_L = 10$ kΩ to V_{EE}; $C_L = 15$ pF to V_{EE}; $\overline{E}$ or S_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value); see Fig. 2.
7. $R_L = 1$ kΩ; $C_L = 5$ pF; channel OFF; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -50$ dB; see Fig. 3.
8. $R_L = 1$ kΩ; $C_L = 5$ pF; channel ON; $V_{is} = ½ V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about $½ V_{DD}$);
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 3.

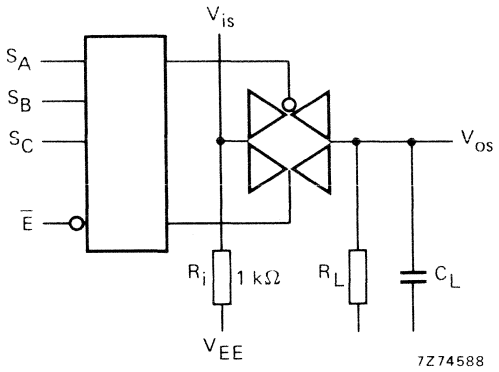


Fig. 2

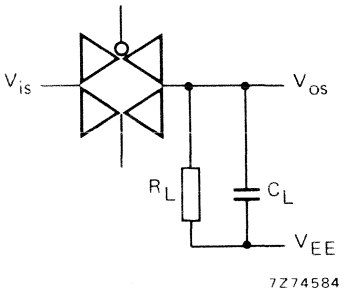
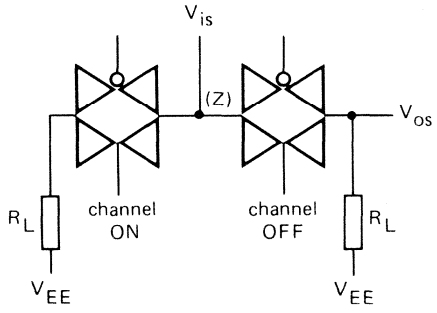
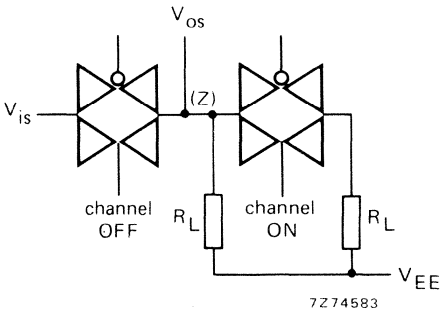


Fig. 3



(a)



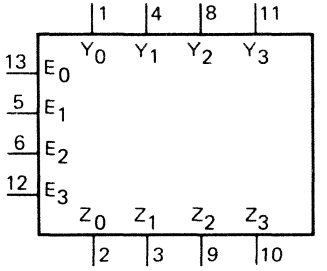
(b)

Fig. 4

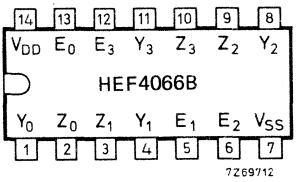
QUADRUPLE BILATERAL SWITCHES

The HEF4066B has four independent bilateral analogue switches (transmission gates). Each switch has two input/output terminals (Y/Z) and an active HIGH enable input (E). A HIGH on E establishes a low impedance bidirectional path between Y and Z (ON condition). A LOW on E disables the switch and establishes a high impedance between Y and Z (OFF condition).

The HEF4066B is pin compatible with the HEF4016B but exhibits a much lower ON resistance. In addition the ON resistance is relatively constant over the full input signal range.



7Z69571.1



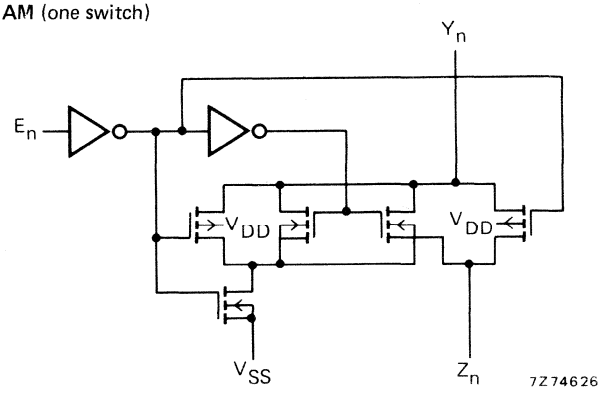
7Z69712

HEF4016BP: 14-lead DIL; plastic (SOT-27).
HEF4016BD: 14-lead DIL; ceramic (SOT-73).

PINNING

E_0 to E_3 enable inputs
Y_0 to Y_3 input/output terminals
Z_0 to Z_3 input/output terminals

LOGIC DIAGRAM (one switch)



7Z74626

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	350	1050	Ω	E_n at V_{DD}; V_i = V_{SS} to V_{DD}; see Fig.1
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	E_n at V_{DD}; V_i = V_{SS}; see Fig.1
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	E_n at V_{DD}; V_i = V_{DD}; see Fig.1
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	15	–	Ω	E_n at V_{DD}; V_i = V_{SS} to V_{DD}; see Fig.1
	10		10	–	Ω	
	15		5	–	Ω	
OFF state leakage current, any channel OFF	5	I_{OZ}	–	–	nA	E_n at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

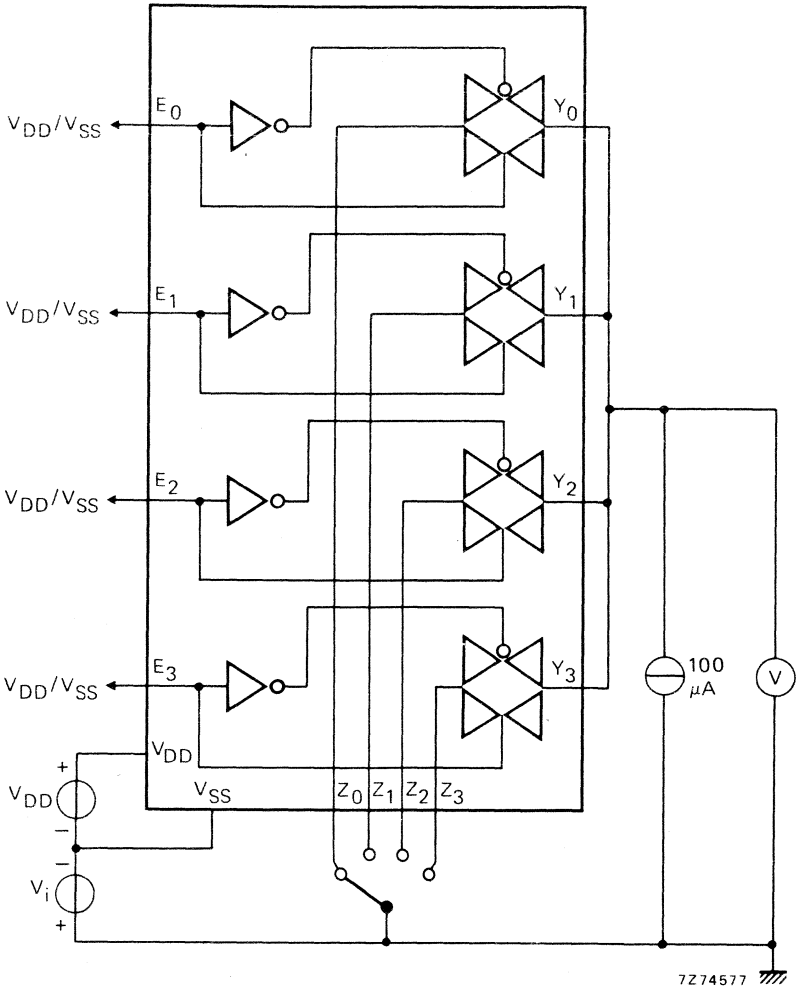


Fig.1 Test set-up for measuring R_{ON}.

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$	5		10	20	ns	
HIGH to LOW	10	t_{PHL}	5	10	ns	note 1
	15		5	10	ns	
	5		10	20	ns	
LOW to HIGH	10	t_{PLH}	5	10	ns	note 1
	15		5	10	ns	
Output disable times						
$E_n \rightarrow V_{os}$	5		80	160	ns	
HIGH	10	t_{PHZ}	65	130	ns	note 2
	15		60	120	ns	
	5		80	160	ns	
LOW	10	t_{PLZ}	70	140	ns	note 2
	15		70	140	ns	
Output enable times						
$E_n \rightarrow V_{os}$	5		40	80	ns	
HIGH	10	t_{PZH}	20	40	ns	note 2
	15		15	30	ns	
	5		45	90	ns	
LOW	10	t_{PZL}	20	40	ns	note 2
	15		15	30	ns	
Distortion, sine-wave	5		0,25		%	
response	10		0,04		%	note 3
	15		0,04		%	
Crosstalk between	5		–		MHz	
any two channels	10		1		MHz	note 4
	15		–		MHz	
Crosstalk; enable	5		–		mV	
input to output	10		50		mV	note 5
	15		–		mV	
OFF-state	5		–		MHz	
feed-through	10		1		MHz	note 6
	15		–		MHz	
ON-state frequency	5		–		MHz	
response	10		90		MHz	note 7
	15		–		MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; E_n at V_{DD}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; E_n is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} at V_{SS} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
3. R_L = 10 kΩ; C_L = 15 pF; E_n at V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig. 3.
4. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}\,(B)}{V_{is}\,(A)}$ = −50 dB; E_n (A) at V_{SS}; E_n (B) at V_{DD}; see Fig. 4.
5. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; E_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value);
   see Fig. 2.
6. R_L = 1 kΩ; C_L = 5 pF; E_n at V_{SS}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −50 dB; see Fig. 3.
7. R_L = 1 kΩ; C_L = 5 pF; E_n at V_{DD}; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}}$ = −3 dB; see Fig. 3.

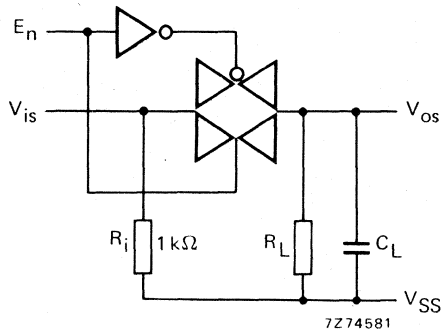


Fig.2

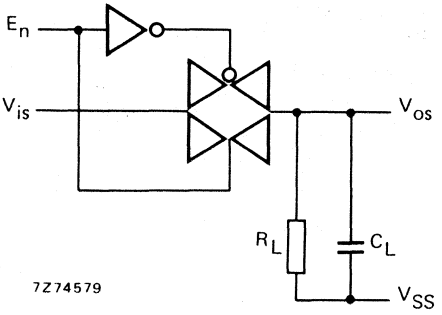
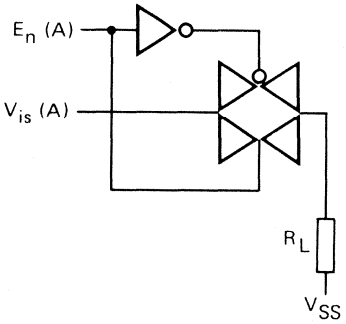
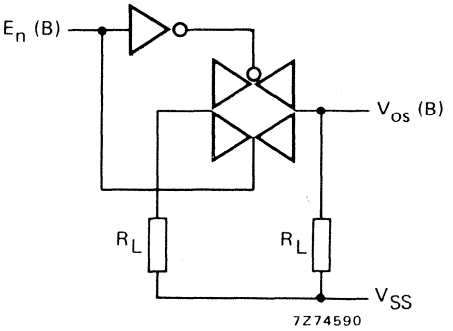


Fig.3



(a)



(b)

Fig.4

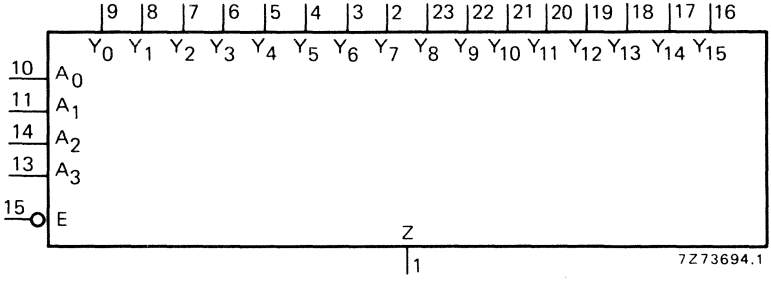
16-CHANNEL ANALOGUE MULTIPLEXER/DEMULTIPLEXER

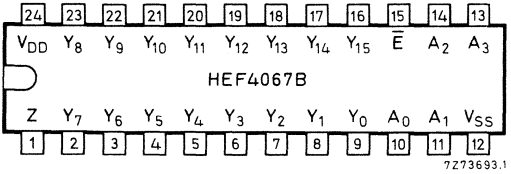
The HEF4067B is a 16-channel analogue multiplexer/demultiplexer with four address inputs (A_0 to A_3), an active LOW enable input ($\overline{E}$), sixteen independent inputs/outputs (Y_0 to Y_{15}) and a common input/output (Z).

The device contains sixteen bidirectional analogue switches, each with one side connected to an independent input/output (Y_0 to Y_{15}) and the other side connected to the common input/output (Z).

With $\overline{E}$ LOW, one of the sixteen switches is selected (low impedance ON-state) by A_0 to A_3. All unselected switches are in the high impedance OFF-state. With $\overline{E}$ HIGH all switches are in the high impedance OFF-state, independent of A_0 to A_3.

The analogue inputs/outputs (Y_0 to Y_{15} and Z) can swing between V_{DD} as a positive limit and V_{SS} as a negative limit. $V_{DD} - V_{SS}$ may not exceed 15 V.





HEF4067BP: 24-lead DIL; plastic (SOT-101A).

HEF4067BD: 24-lead DIL; ceramic (SOT-94).

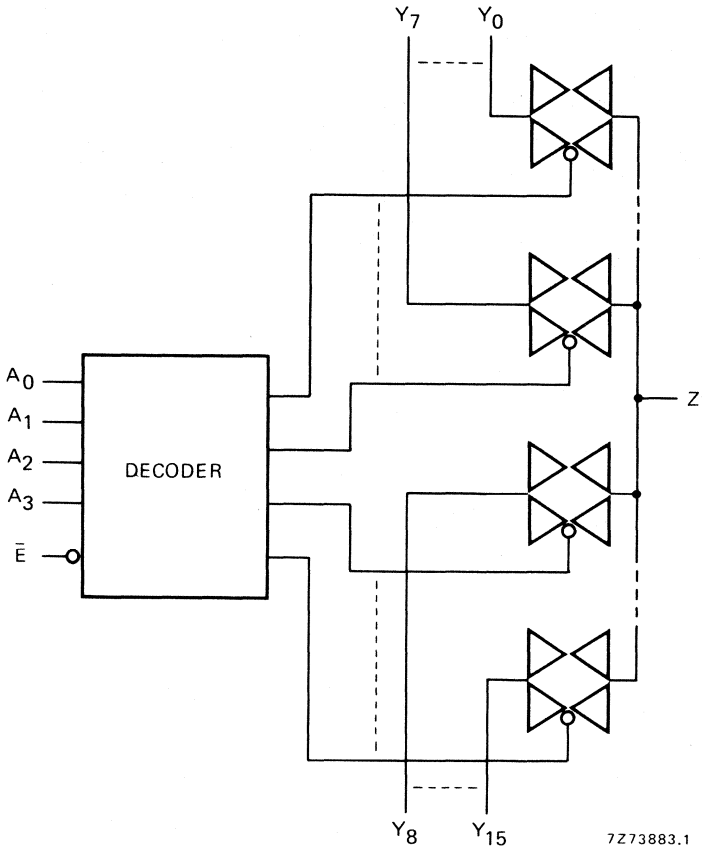
PINNING

Y_0 to Y_{15}	independent inputs/outputs
A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
Z	common input/output

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs					channel
$\overline{E}$	A_3	A_2	A_1	A_0	ON
L	L	L	L	L	$Y_0 - Z$
L	L	L	L	H	$Y_1 - Z$
L	L	L	H	L	$Y_2 - Z$
L	L	L	H	H	$Y_3 - Z$
L	L	H	L	L	$Y_4 - Z$
L	L	H	L	H	$Y_5 - Z$
L	L	H	H	L	$Y_6 - Z$
L	L	H	H	H	$Y_7 - Z$
L	H	L	L	L	$Y_8 - Z$
L	H	L	L	H	$Y_9 - Z$
L	H	L	H	L	$Y_{10} - Z$
L	H	L	H	H	$Y_{11} - Z$
L	H	H	L	L	$Y_{12} - Z$
L	H	H	L	H	$Y_{13} - Z$
L	H	H	H	L	$Y_{14} - Z$
L	H	H	H	H	$Y_{15} - Z$
H	X	X	X	X	none

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

NOTE

To avoid drawing V_{DD} current out of terminal Z, when switch current flows into terminals Y, the voltage drop across the bidirectional switch must not exceed 0,4 V. If the switch current flows into terminal Z, no V_{DD} current will flow out of terminals Y.

D.C. CHARACTERISTICS

T_{amb} = 25 °C

	V_{DD} V	symbol	typ	max		conditions
ON resistance	5	R_{ON}	350	1050	Ω	V_i = 0 to V_{DD} see Fig.1
	10		80	245	Ω	
	15		60	175	Ω	
ON resistance	5	R_{ON}	115	340	Ω	V_i = 0 see Fig.1
	10		50	160	Ω	
	15		40	115	Ω	
ON resistance	5	R_{ON}	120	365	Ω	V_i = V_{DD} see Fig.1
	10		65	200	Ω	
	15		50	155	Ω	
'Δ' ON resistance between any two channels	5	ΔR_{ON}	15	–	Ω	V_i = 0 to V_{DD} see Fig.1
	10		10	–	Ω	
	15		5	–	Ω	
OFF-state leakage current, all channels OFF	5	I_{OZZ}	–	–	nA	$\overline{E}$ at V_{DD}
	10		–	–	nA	
	15		–	1000	nA	
OFF-state leakage current, any channel	5	I_{OZY}	–	–	nA	$\overline{E}$ at V_{SS}
	10		–	–	nA	
	15		–	200	nA	

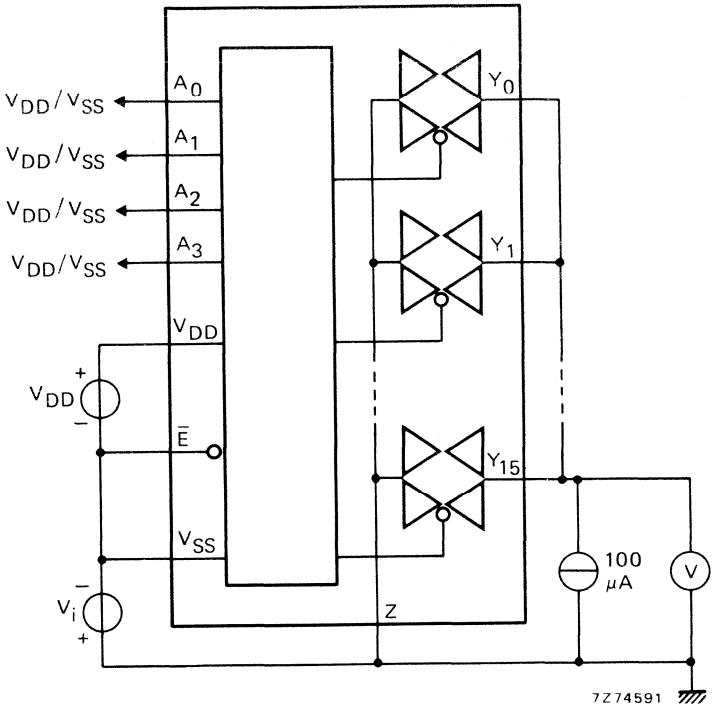


Fig. 1 Test set-up for measuring R_{ON}.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$13\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		
Propagation delays						
$V_{is} \rightarrow V_{os}$ HIGH to LOW	5	t_{PHL}	30	60	ns	note 1
	10		15	25	ns	
	15		10	20	ns	
LOW to HIGH	5	t_{PLH}	25	50	ns	note 1
	10		10	20	ns	
	15		10	20	ns	
$A_n \rightarrow V_{os}$ HIGH to LOW	5	t_{PHL}	190	380	ns	note 2
	10		70	145	ns	
	15		50	100	ns	
LOW to HIGH	5	t_{PLH}	175	345	ns	note 2
	10		70	140	ns	
	15		50	100	ns	
Output disable times						
$\overline{E}_n \rightarrow V_{os}$ HIGH	5	t_{PHZ}	195	385	ns	note 3
	10		140	280	ns	
	15		130	260	ns	
LOW	5	t_{PLZ}	215	435	ns	note 3
	10		180	355	ns	
	15		170	340	ns	
Output enable times						
$\overline{E}_n \rightarrow V_{os}$ HIGH	5	t_{PZH}	155	315	ns	note 3
	10		70	135	ns	
	15		50	100	ns	
LOW	5	t_{PZL}	170	340	ns	note 3
	10		70	140	ns	
	15		50	100	ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max	
Distortion, sine-wave response	5		0,25	%	note 4
	10		0,04	%	
	15		0,04	%	
Crosstalk between any two channels	5		–	MHz	note 5
	10		1	MHz	
	15		–	MHz	
Crosstalk; enable or address input to output	5		–	mV	note 6
	10		50	mV	
	15		–	mV	
OFF-state feed-through	5		–	MHz	note 7
	10		1	MHz	
	15		–	MHz	
ON-state frequency response	5		13	MHz	note 8
	10		40	MHz	
	15		70	MHz	

NOTES

V_{is} is the input voltage at a Y or Z terminal, whichever is assigned as input.
V_{os} is the output voltage at a Y or Z terminal, whichever is assigned as output.

1. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; $\overline{E}$ at V_{SS}; V_{is} is V_{DD} (square-wave); see Fig. 2.
2. R_L = 10 kΩ to V_{SS}; C_L = 50 pF to V_{SS}; $\overline{E}$ at V_{SS}; A_n is V_{DD} (square-wave); see Fig. 2.
3. R_L = 10 kΩ; C_L = 50 pF to V_{SS}; $\overline{E}$ is V_{DD} (square-wave);
   V_{is} at V_{DD} and R_L at V_{SS} for t_{PHZ} and t_{PZH};
   V_{is} at V_{SS} and R_L at V_{DD} for t_{PLZ} and t_{PZL}; see Fig. 2.
4. R_L = 10 kΩ; C_L = 15 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   f_{is} = 1 kHz; see Fig. 3.
5. R_L = 1 kΩ; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -40$ dB; see Fig. 4.
6. R_L = 10 kΩ to V_{SS}; C_L = 15 pF to V_{SS}; $\overline{E}$ or A_n is V_{DD} (square-wave); crosstalk is V_{os} (peak value); see Fig. 2.
7. R_L = 1 kΩ; C_L = 5 pF; channel OFF; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -40$ dB; see Fig. 3.
8. R_L = 1 kΩ; C_L = 5 pF; channel ON; V_{is} = ½ $V_{DD(p\text{-}p)}$ (sine-wave, symmetrical about ½ V_{DD});
   $20 \log \frac{V_{os}}{V_{is}} = -3$ dB; see Fig. 3.

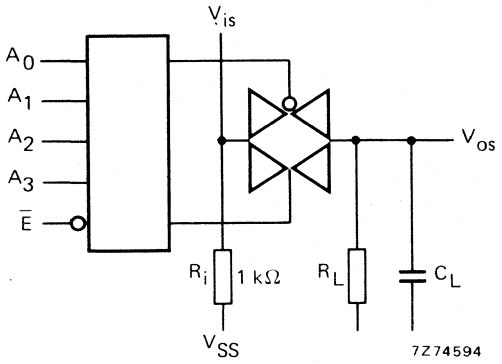


Fig. 2

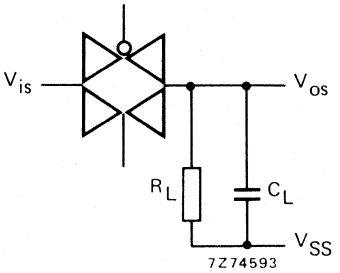


Fig. 3

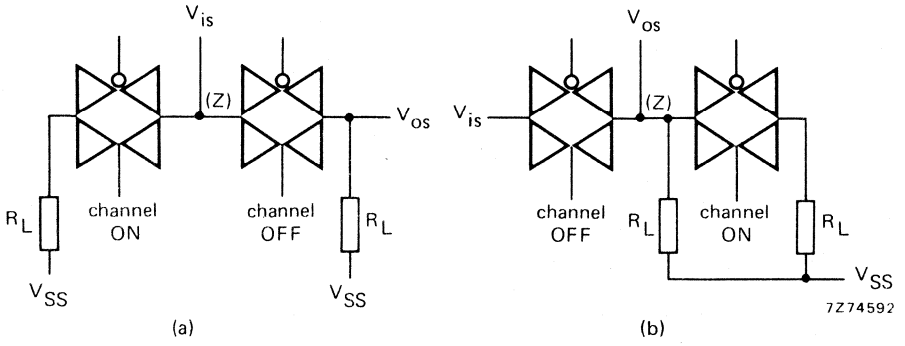
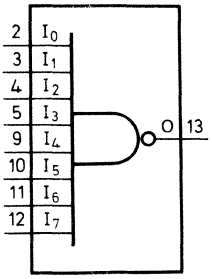
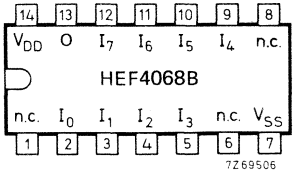


Fig. 4

8-INPUT NAND GATE

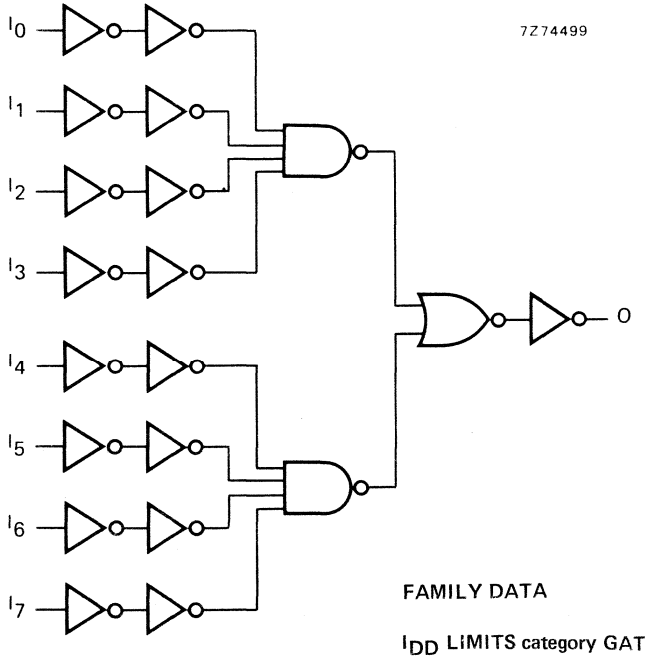
The HEF4068B provides the 8-input NAND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4068BP: 14-lead DIL: plastic (SOT-27).
HEF4068BD: 14-lead DIL: ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA

I_{DD} LIMITS category GATES

} see Family Specifications

A.C. CHARACTERISTICS

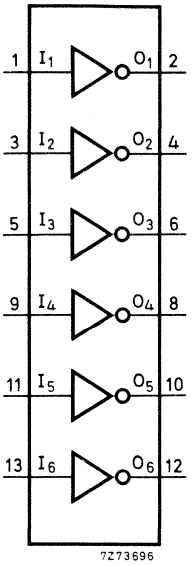
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

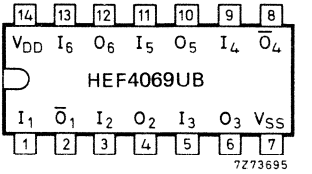
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O$	5		95	195	ns	68 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	40	85	ns	29 ns + (0,23 ns/pF)C_L
	15		30	65	ns	22 ns + (0,16 ns/pF)C_L
	5		80	165	ns	53 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF)C_L
	15		30	60	ns	22 ns + (0,16 ns/pF)C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

HEX INVERTER

The HEF4069UB is a general purpose hex inverter which has standard input and output characteristics. A single-stage design has been used since the output impedance of a single-input gate is not pattern sensitive.





HEF4069UBP : 14-lead DIL; plastic (SOT-27).
HEF4069UBD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM

Identical to the one above.

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Input voltage HIGH	5	V_{IH}	4,0	–	4,0	–	4,0	–	V
	10		8,0	–	8,0	–	8,0	–	V
	15		12,5	–	12,5	–	12,5	–	V
Input voltage LOW	5	V_{IL}	–	1,0	–	1,0	–	1,0	V
	10		–	2,0	–	2,0	–	2,0	V
	15		–	2,5	–	2,5	–	2,5	V

A.C. CHARACTERISTICS

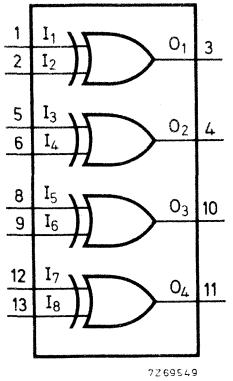
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

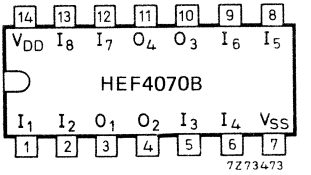
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW	5	t_{PHL}	45	90	ns	18 ns + (0,55 ns/pF) C_L
	10		20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	25	ns	7 ns + (0,16 ns/pF) C_L
LOW to HIGH	5	t_{PLH}	40	80	ns	13 ns + (0,55 ns/pF) C_L
	10		20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$4\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$17\,700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

QUADRUPLE EXCLUSIVE-OR GATE

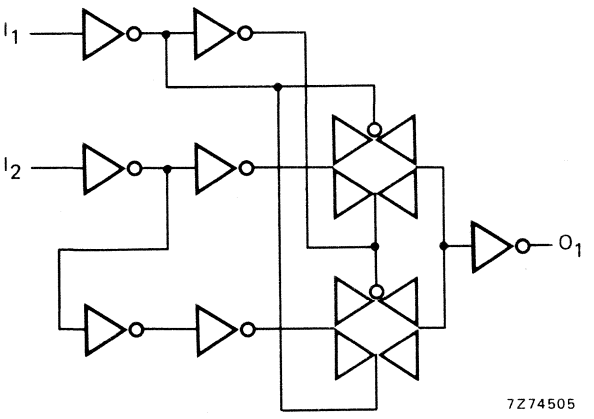
The HEF4070B provides the positive quadruple exclusive-OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4070BP : 14-lead DIL; plastic (SOT-27).
HEF4070BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



TRUTH TABLE

I_1	I_2	O_1
L	L	L
H	L	H
L	H	H
H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

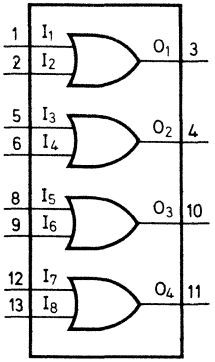
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		85	175	ns	57 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	75	ns	23 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		75	150	ns	47 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	65	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

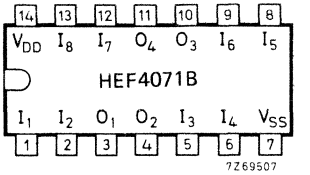
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$14\,400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT OR GATE

The HEF4071B is a positive logic quadruple 2-input OR gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



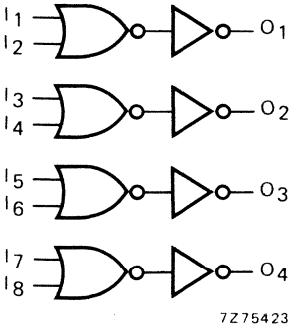
7Z69551



7Z69507

HEF4071BP: 14-lead DIL; plastic (SOT-27).
HEF4071BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



7Z75423

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

A.C. CHARACTERISTICS

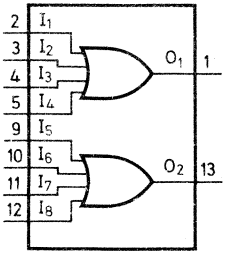
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transistion times ⩽ 20 ns

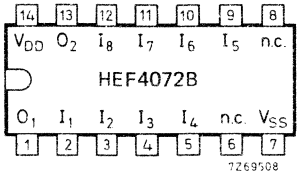
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	115	ns	28 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	15 ns + (0,23 ns/pF) C_L
	15		20	35	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	18 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	45	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1150 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	19 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 4-INPUT OR GATE

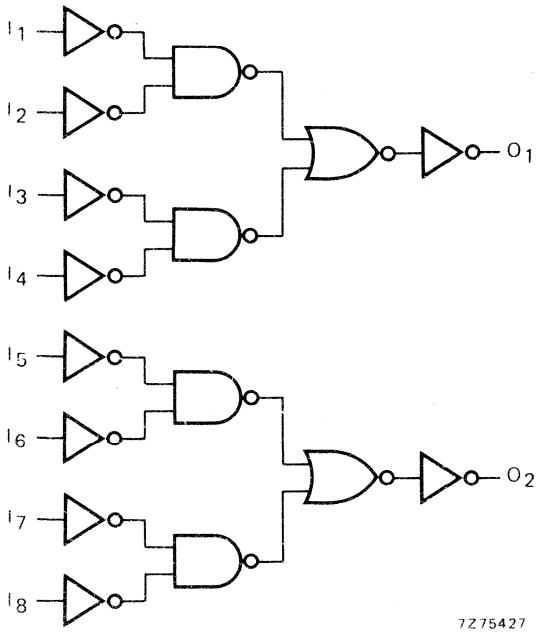
The HEF4072B provides the positive dual 4-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4072BP: 14-lead DIL; plastic (SOT-27).
HEF4072BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA	see Family Specifications
I_{DD} LIMITS category GATES	

A.C. CHARACTERISTICS

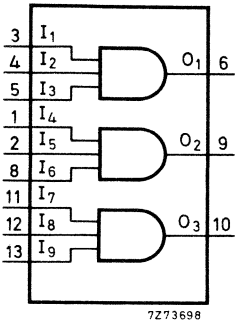
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

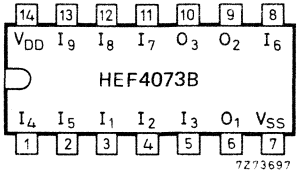
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		80	155	ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	55	ns	17 ns + (0,16 ns/pF) C_L
	5		75	145	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	55	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	950 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	13 700 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

TRIPLE 3-INPUT AND GATE

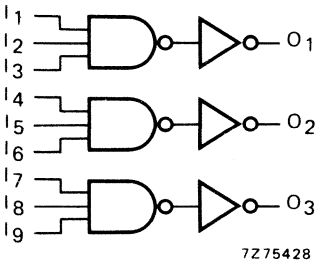
The HEF4073B provides the positive triple 3-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4073BP: 14-lead DIL; plastic (SOT-27).
HEF4073BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

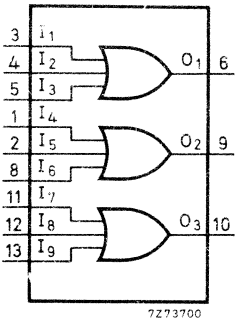
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

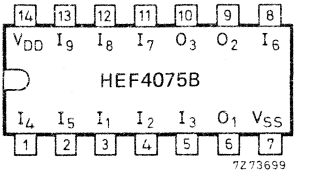
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	110	ns	23 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		45	90	ns	13 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	600 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	8400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

TRIPLE 3-INPUT OR GATE

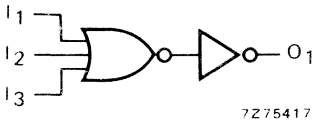
The HEF4075B provides the positive triple 3-input OR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4075BP: 14-lead DIL; plastic (SOT-27).
HEF4075BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



FAMILY DATA

I_{DD} **LIMITS category GATES** | see Family Specifications

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

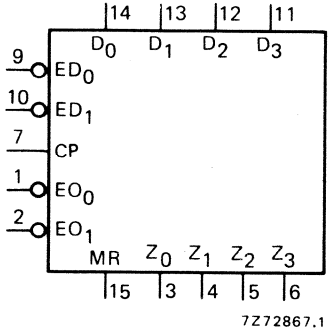
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \longrightarrow O_n$	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		65	130	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

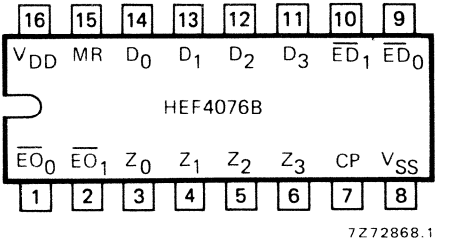
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	750 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	3 600 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	11 200 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

QUADRUPLE D-TYPE REGISTER WITH 3-STATE OUTPUTS

The HEF4076B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), two active LOW data enable inputs ($\overline{ED}_0$ and $\overline{ED}_1$), a common clock input (CP), four 3-state outputs (Z_0 to Z_3), two active LOW output enable inputs ($\overline{EO}_0$ and $\overline{EO}_1$), and an overriding asynchronous master reset input (MR).

Information on D_0 to D_3 is stored in the four flip-flops on the LOW to HIGH transition of CP if both $\overline{ED}_0$ and $\overline{ED}_1$ are LOW. A HIGH on either $\overline{ED}_0$ or $\overline{ED}_1$ prevents the flip-flops from changing on the LOW to HIGH transition of CP, independent of the information on D_0 to D_3. When both $\overline{EO}_0$ and $\overline{EO}_1$ are LOW, the contents of the four flip-flops are available at Z_0 to Z_3. A HIGH on either $\overline{EO}_0$ or $\overline{EO}_1$ forces Z_0 to Z_3 into the high impedance OFF-state. A HIGH on MR resets all four flip-flops, independent of all other input conditions.





HEF4076BP : 16-lead DIL; plastic (SOT-38Z).
HEF4076BD: 16-lead DIL; ceramic (SOT-74).

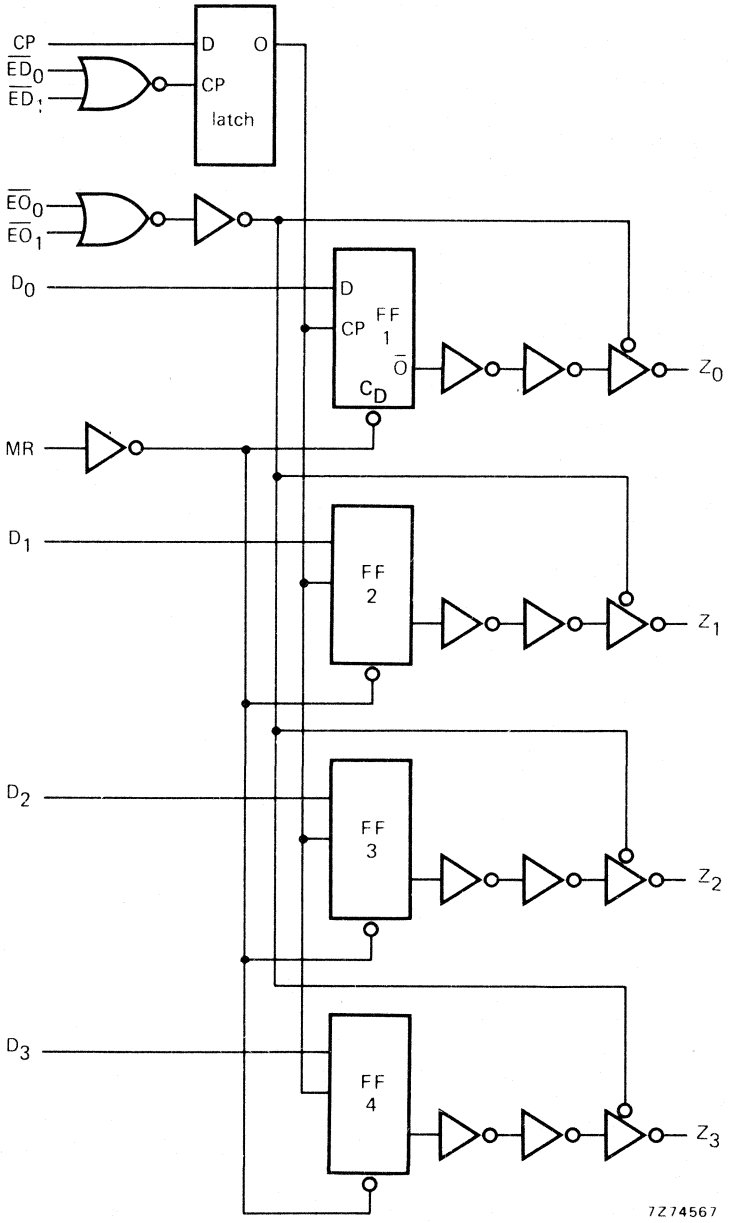
PINNING

D_0 to D_3	data inputs
$\overline{ED}_0$, $\overline{ED}_1$	data enable inputs (active LOW)
$\overline{EO}_0$, $\overline{EO}_1$	output enable inputs (active LOW)
CP	clock input (LOW to HIGH, edge-triggered)
MR	master reset input
Z_0 to Z_3	data outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs					outputs
MR	CP	$\overline{ED}_0$	$\overline{ED}_1$	D_n	Z_n
H	X	X	X	X	L
L	∫	H	X	X	no change
L	∫	X	H	X	no change
L	∫	L	L	H	H
L	∫	L	L	L	L
L	∖	X	X	X	no change

$\overline{EO}_0 = \overline{EO}_1$ = LOW

When either $\overline{EO}_0$ or $\overline{EO}_1$ is HIGH, the outputs are disabled (high impedance).

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
∖ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

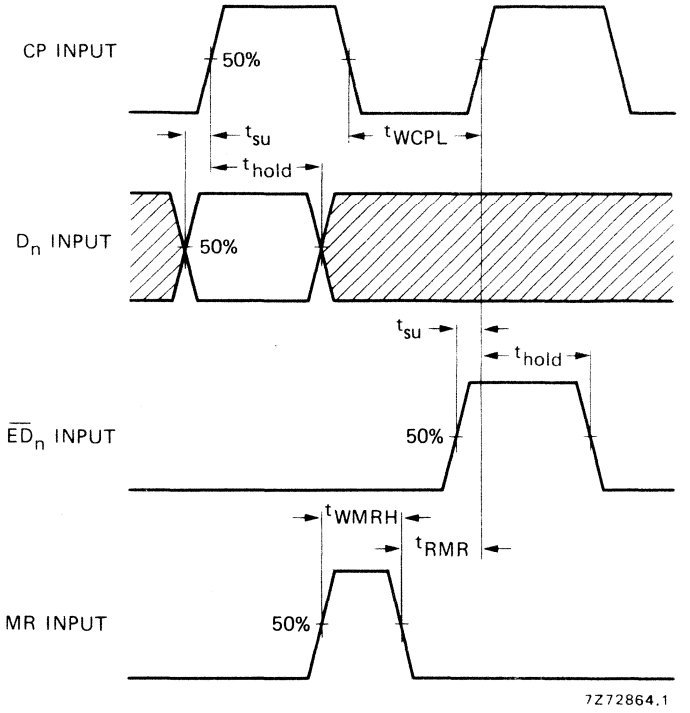
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP → Z_n	5			150	305 ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
MR → Z_n	5			95	190 ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
Output disable times						
$\overline{EO}_n$ → Z_n	5			50	105 ns	
HIGH	10	t_{PHZ}		35	70 ns	
	15			30	65 ns	
	5			45	90 ns	
LOW	10	t_{PLZ}		30	65 ns	
	15			30	60 ns	
Output enable times						
$\overline{EO}_n$ → Z_n	5			65	130 ns	
HIGH	10	t_{PZH}		30	55 ns	
	15			20	40 ns	
	5			60	120 ns	
LOW	10	t_{PZL}		25	50 ns	
	15			20	35 ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Set-up times	5		10	−15		ns	
$D_n \rightarrow CP$	10	t_{su}	0	−10		ns	
	15		0	−5		ns	
	5		0	−50		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{su}	0	−20		ns	
	15		0	−15		ns	
Hold times	5		55	30		ns	
$D_n \rightarrow CP$	10	t_{hold}	20	10		ns	
	15		15	10		ns	
	5		25	−25		ns	
$\overline{ED}_n \rightarrow CP$	10	t_{hold}	10	−10		ns	
	15		5	−5		ns	see also waveforms on page 5
Minimum clock pulse width; LOW	5		120	60		ns	
	10	t_{WCPL}	45	20		ns	
	15		30	15		ns	
Minimum MR pulse width; HIGH	5		55	25		ns	
	10	t_{WMRH}	30	15		ns	
	15		20	10		ns	
Recovery time for MR	5		90	45		ns	
	10	t_{RMR}	35	15		ns	
	15		20	10		ns	
Maximum clock pulse frequency	5		4	8		MHz	
	10	f_{max}	11	22		MHz	
	15		16	32		MHz	

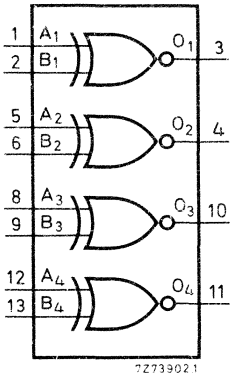
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$9300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$24\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

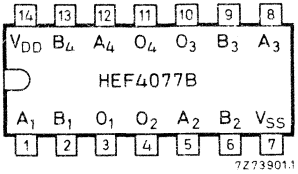


Waveforms showing minimum CP and MR pulse widths, set-up and hold times for D_n to CP and $\overline{ED}_n$ to CP, and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE EXCLUSIVE-NOR GATE

The HEF4077B provides the exclusive-NOR function. The outputs are fully buffered for best performance.





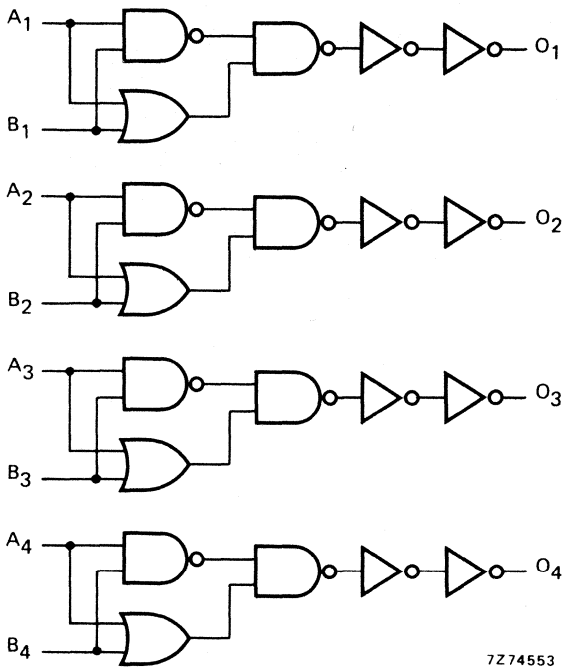
HEF4077BP: 14-lead DIL; plastic (SOT-27).
HEF4077BD: 14-lead DIL; ceramic (SOT-73).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

A_n	B_n	O_n
L	L	H
L	H	L
H	L	L
H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)

A.C. CHARACTERISTICS

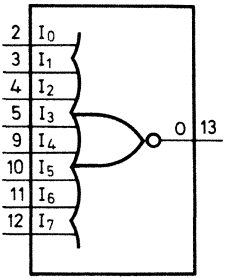
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

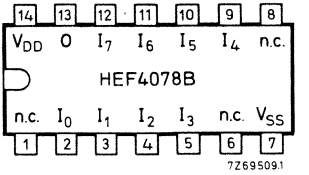
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		75	150	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		30	55	ns	22 ns + (0,16 ns/pF) C_L
	5		70	145	ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	850 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	14 700 f_i + Σ($f_o C_L$) x V_{DD}^2	

8-INPUT NOR GATE

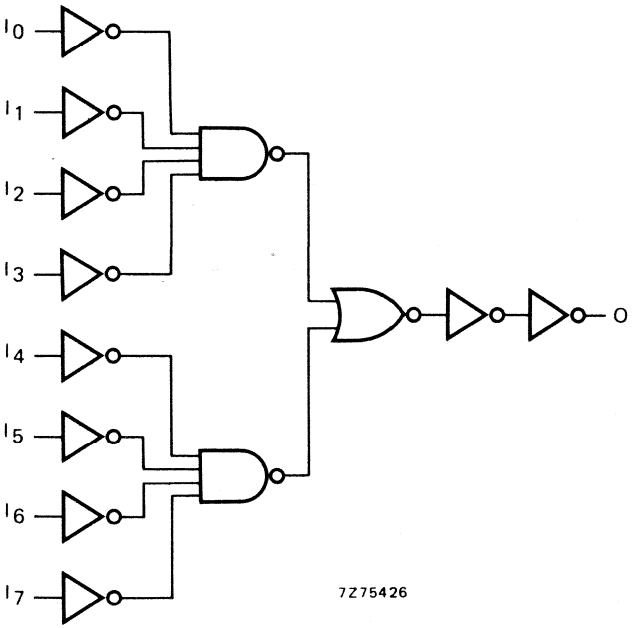
The HEF4078B provides the positive 8-input NOR function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4078BP: 14-lead DIL; plastic (SOT-27).
HEF4078BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

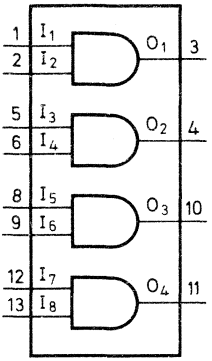
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$						
HIGH to LOW	5	t_{PHL}	80	160	ns	53 ns + (0,55 ns/pF) C_L
	10		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
	5		80	160	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L

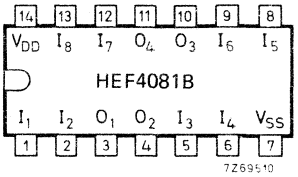
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$750\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

QUADRUPLE 2-INPUT AND GATE

The HEF4081B provides the positive quadruple 2-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.



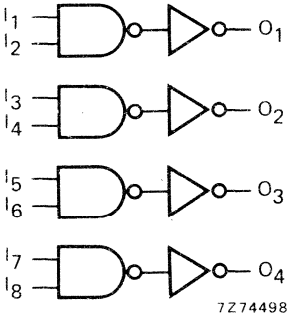
7Z69569



7Z69510

HEF4081BP: 14-lead DIL; plastic (SOT-27).
HEF4081BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM



7Z74498

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

A.C. CHARACTERISTICS

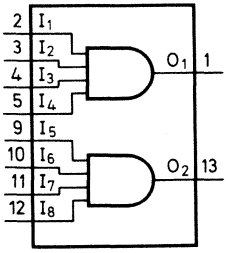
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

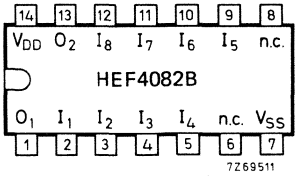
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		55	110	ns	28 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	25	50	ns	14 ns + (0,23 ns/pF)C_L
	15		20	40	ns	12 ns + (0,16 ns/pF)C_L
	5		45	90	ns	18 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	20	40	ns	9 ns + (0,23 ns/pF)C_L
	15		15	30	ns	7 ns + (0,16 ns/pF)C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	800 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	4100 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	
	15	14 700 f_i + $\Sigma(f_oC_L)$ x V_{DD}^2	

DUAL 4-INPUT AND GATE

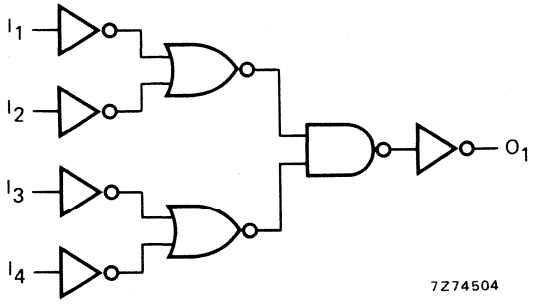
The HEF4082B provides the positive dual 4-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





HEF4082BP : 14-lead DIL; plastic (SOT-27).
HEF4082BD : 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM (one gate)



FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

A.C. CHARACTERISTICS

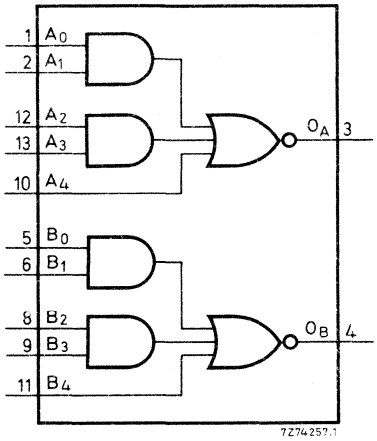
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

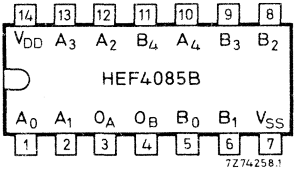
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays $I_n \rightarrow O_n$	5	t_{PHL}; t_{PLH}	65	125	ns	38 ns + (0,55 ns/pF) C_L
	10		30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		25	45	ns	17 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE

The HEF4085B is a dual 2-wide 2-input AND-OR-invert gate, each with an additional input (A_4 or B_4) which can be used as either an expander input or an inhibit input. A HIGH on A_4 or B_4 forces the output (O_A or O_B) LOW independent of the other inputs (A_0 to A_3 or B_0 to B_3). The outputs O_A and O_B are fully buffered for highest noise immunity and pattern insensitivity of output impedance.





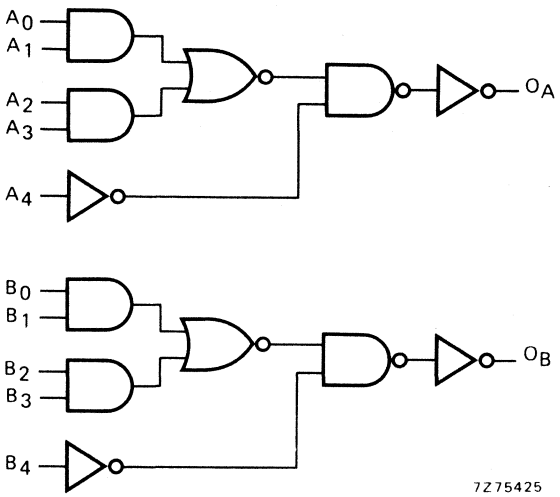
HEF4085BP : 14-lead DIL; plastic (SOT-27).
HEF4085BD: 14-lead DIL; ceramic (SOT-73).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

LOGIC DIAGRAM



LOGIC FUNCTION

$O_A = \overline{A_0 \cdot A_1 + A_2 \cdot A_3 + A_4}$

$O_B = \overline{B_0 \cdot B_1 + B_2 \cdot B_3 + B_4}$

A.C. CHARACTERISTICS

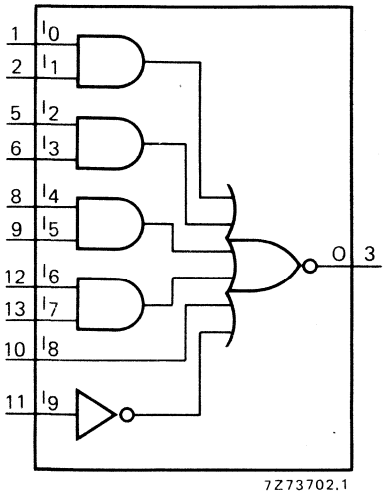
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L
	5		65	135	ns	38 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	55	ns	19 ns + (0,23 ns/pF) C_L
	15		20	40	ns	12 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	750 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	3200 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	9200 f_i + Σ($f_o C_L$) x V_{DD}^2	

4-WIDE 2-INPUT AND-OR-INVERT GATE

The HEF4086B is a 4-wide 2-input AND-OR-invert (AOI) gate with two additional inputs (I_8 and I_9) which can be used as either expander or inhibit inputs by connecting them to any standard LOCMOS output. A HIGH on I_8 or a LOW on I_9 forces the output (O) LOW independent of the other eight inputs (I_0 to I_7). The output (O) is fully buffered for highest noise immunity and pattern insensitivity of output impedance.



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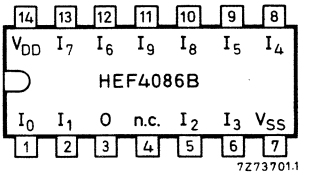

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HEF4086BP: 14-lead DIL; plastic (SOT-27).
HEF4086BD: 14-lead DIL; ceramic (SOT-73).

PINNING

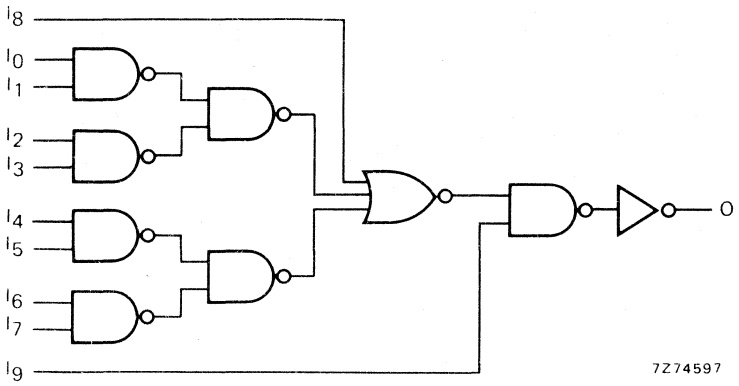
I_0 to I_8	gate inputs
I_9	gate input (active LOW)
O	output (active LOW)

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

LOGIC DIAGRAM



LOGIC FUNCTION

$$O = \overline{I_0 \cdot I_1 + I_2 \cdot I_3 + I_4 \cdot I_5 + I_6 \cdot I_7 + I_8 + \overline{I}_9}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

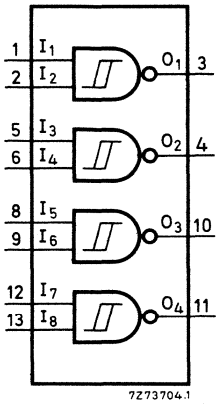
	V_{DD} V	symbol	typ	max	
Propagation delays					
I_0-I_7 → O	5		100		ns
HIGH to LOW	10	t_{PHL}	40		ns
	15		25		ns
	5		100		ns
LOW to HIGH	10	t_{PLH}	40		ns
	15		25		ns
I_8 → O	5		80		ns
HIGH to LOW	10	t_{PHL}	35		ns
	15		20		ns
	5		80		ns
LOW to HIGH	10	t_{PLH}	35		ns
	15		20		ns
I_9 → O	5		65		ns
HIGH to LOW	10	t_{PHL}	35		ns
	15		20		ns
	5		65		ns
LOW to HIGH	10	t_{PLH}	35		ns
	15		20		ns

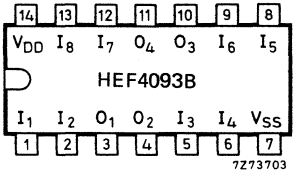
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	800 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	3200 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	9200 f_i + Σ($f_o C_L$) x V_{DD}^2	

DEVELOPMENT SAMPLE DATA

QUADRUPLE 2-INPUT NAND SCHMITT TRIGGER

The HEF4093B consists of four Schmitt-trigger circuits. Each circuit functions as a two-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive voltage (V_{IH}) and the negative voltage (V_{IL}) is defined as hysteresis voltage (V_H).





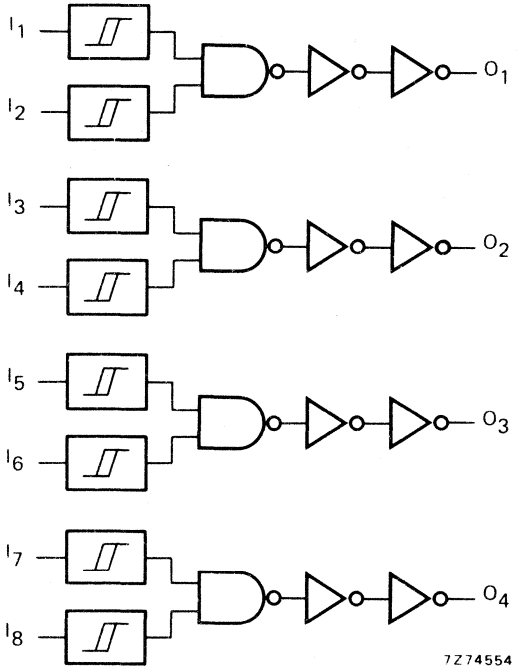
HEF4093BP: 14-lead DIL; plastic (SOT-27).
HEF4093BD: 14-lead DIL; ceramic (SOT-73).

FAMILY DATA

I_{DD} LIMITS category GATES

see Family Specifications

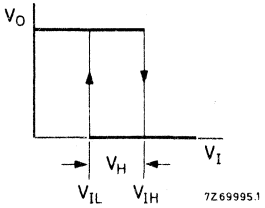
LOGIC DIAGRAM



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C)									
			−40			+25			+85			
			min	typ	max	min	typ	max	min	typ	max	
Hysteresis voltage	5	V_H					0,3					V
	10						0,5					V
	15						0,7					V



Transfer characteristic

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

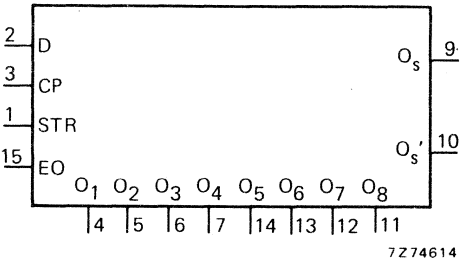
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays	5		90	185	ns	63 ns + (0,55 ns/pF) C_L
$I_n \rightarrow O_n$	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF) C_L
HIGH to LOW	15		30	60	ns	22 ns + (0,16 ns/pF) C_L
	5		85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF) C_L
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L

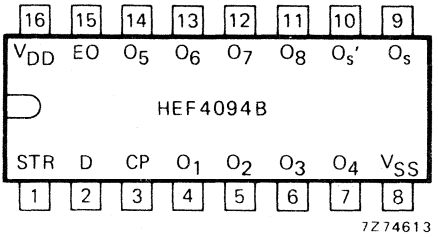
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1300 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6400 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	18 700 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

8-STAGE SHIFT-AND-STORE BUS REGISTER

The HEF4094B is an 8-stage serial shift register having a storage latch associated with each stage for strobing data from the serial input to parallel buffered 3-state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive-going clock transitions. The data in each shift register stage is transferred to the storage register when the strobe (STR) input is HIGH. Data in the storage register appears at the outputs whenever the output enable (EO) signal is HIGH.

Two serial outputs (O_S and O'_S) are available for cascading a number of HEF4094B devices. Data is available at O_S on positive-going clock edges to allow high-speed operation in cascaded systems in which the clock rise time is fast. The same serial information is available at O'_S on the next negative-going clock edge and provides cascading HEF4094B devices when the clock rise time is slow.





HEF4094BP: 16-lead DIL; plastic (SOT-38Z).
HEF4094BD: 16-lead DIL; ceramic (SOT-74).

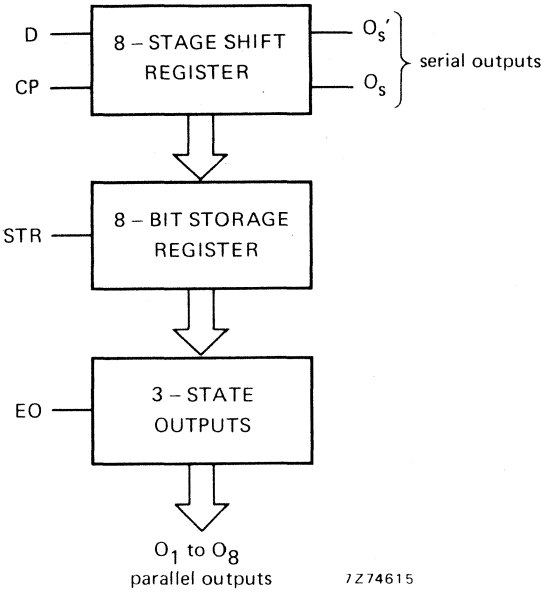
PINNING

D	data input
CP	clock input
STR	strobe input
EO	output enable input
O_S, O'_S	serial outputs
O_1 to O_8	parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

BLOCK DIAGRAM



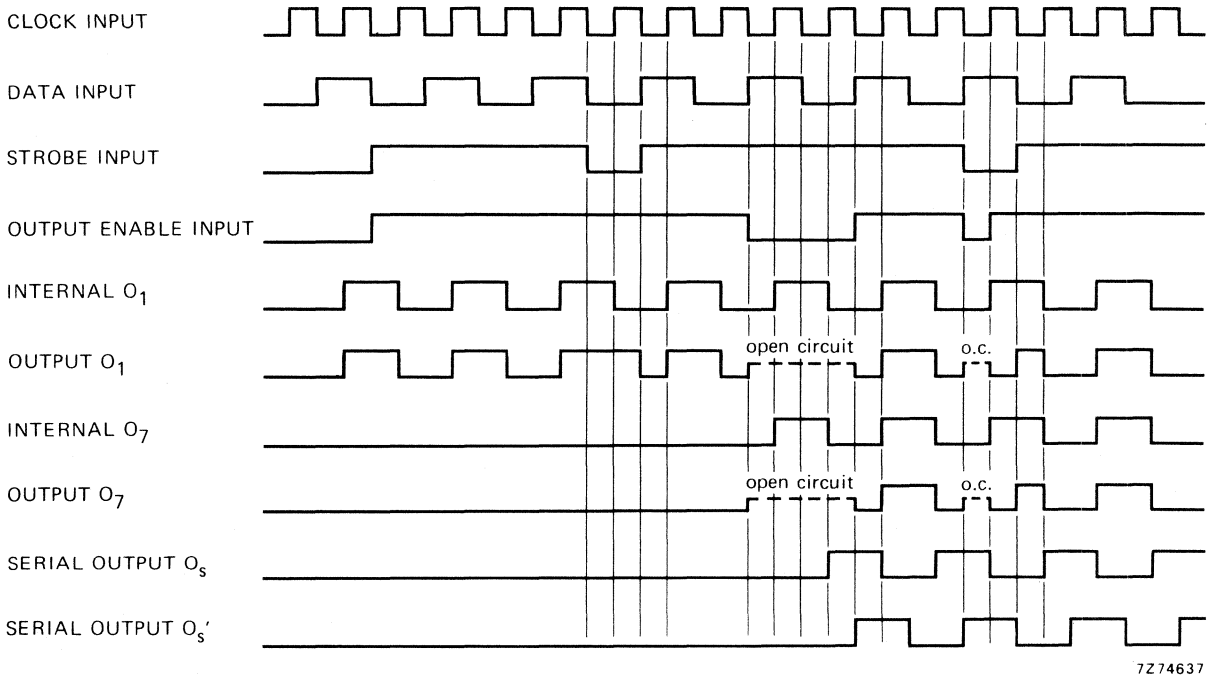
FUNCTION TABLE

inputs				parallel outputs		serial outputs	
CP	EO	STR	D	O_1	O_n	O_s	O_s'
∫	L	X	X	oc	oc	O_7	nc
⌡	L	X	X	oc	oc	nc	O_7
∫	H	L	X	nc	nc	O_7	nc
∫	H	H	L	L	O_{n-1}	O_7	nc
∫	H	H	H	H	O_{n-1}	O_7	nc
⌡	H	H	H	nc	nc	nc	O_7

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌡ = negative-going transition
oc = open circuit
nc = no change

DEVELOPMENT SAMPLE DATA

TIMING DIAGRAM



A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Propagation delays						
CP → O_S, O_S'	5	t_{PLH}, t_{PHL}		180		ns
	10			75		ns
	15			60		ns
CP → O_n	5	t_{PLH}, t_{PHL}		250		ns
	10			120		ns
	15			80		ns
STR → O_n	5	t_{PLH}, t_{PHL}		175		ns
	10			90		ns
	15			60		ns
EO → O_n	5	t_{PLH}, t_{PHL}		85		ns
	10			45		ns
	15			30		ns
Minimum STR pulse width	5	t_{WSTR}		60		ns
	10			25		ns
	15			20		ns
Minimum CP pulse width	5	t_{WCP}		60		ns
	10			35		ns
	15			25		ns
Minimum D set-up time	5	t_{suD}		35		ns
	10			25		ns
	15			15		ns
Maximum clock pulse frequency	5	f_{max}		4		MHz
	10			8		MHz
	15			10		MHz

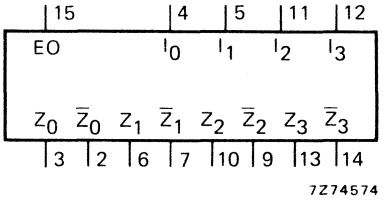
QUADRUPLE LOW TO HIGH VOLTAGE TRANSLATOR WITH 3-STATE OUTPUTS

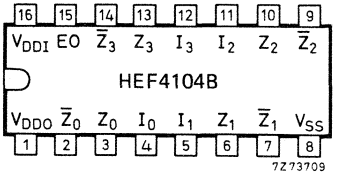
The HEF4104B quadruple low voltage to high voltage translator with 3-state outputs provides the capability of interfacing low voltage circuits to high voltage circuits, such as low voltage LOCMOS and TTL to high voltage LOCMOS. It has four data inputs (I_0 to I_3), an active HIGH output enable input (EO), four data outputs (Z_0 to Z_3) and their complements ($\overline{Z}_0$ to $\overline{Z}_3$).

With EO HIGH, Z_0 to Z_3 and $\overline{Z}_0$ to $\overline{Z}_3$ are in the low impedance ON-state, either HIGH or LOW as determined by I_0 to I_3; with EO LOW, Z_0 to Z_3 and $\overline{Z}_0$ to $\overline{Z}_3$ are in the high impedance OFF-state.

The device uses a common negative supply (V_{SS}) and separate positive supplies for inputs (V_{DDI}) and outputs (V_{DDO}). V_{DDI} must always be less than or equal to V_{DDO}, even during power turn-on and turn-off. For the permissible operating range of V_{DDI} and V_{DDO} see graph on page 4.

Each input protection circuit is terminated between V_{DDO} and V_{SS}. This allows the input signals to be driven from any potential between V_{DDO} and V_{SS}, without regard to current limiting. When driving from potentials greater than V_{DDO} or less than V_{SS}, the current at each input must be limited to 10 mA.





HEF4104BP : 16-lead DIL; plastic (SOT-38Z).
HEF4104BD: 16-lead DIL; ceramic (SOT-74).

PINNING

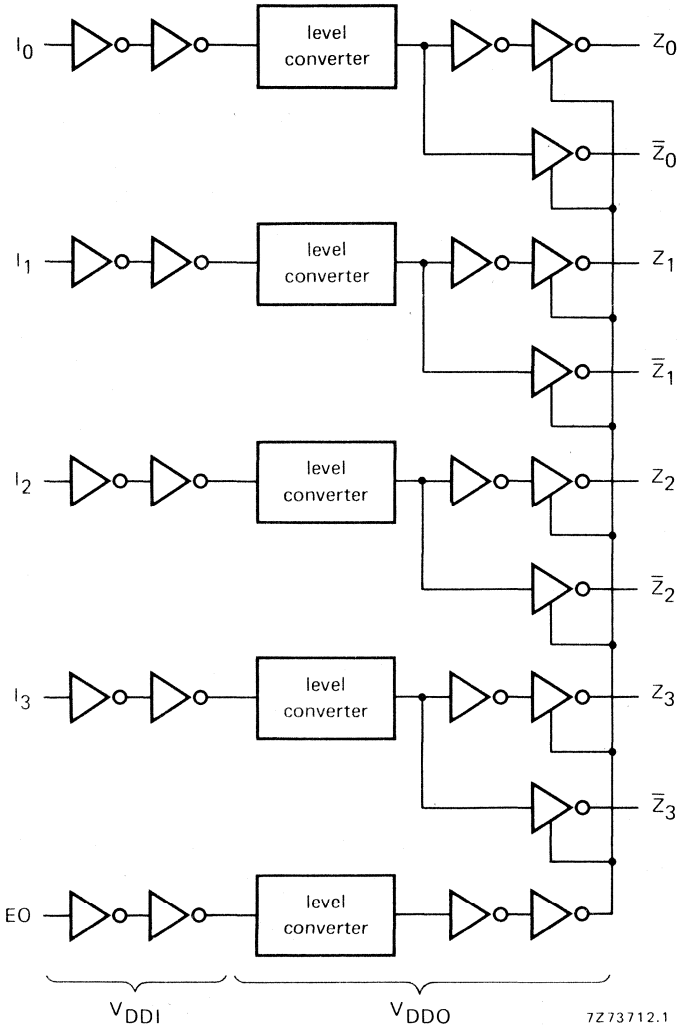
I_0 to I_3	data inputs
EO	output enable input
Z_0 to Z_3	data outputs
$\overline{Z}_0$ to $\overline{Z}_3$	complementary data outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM

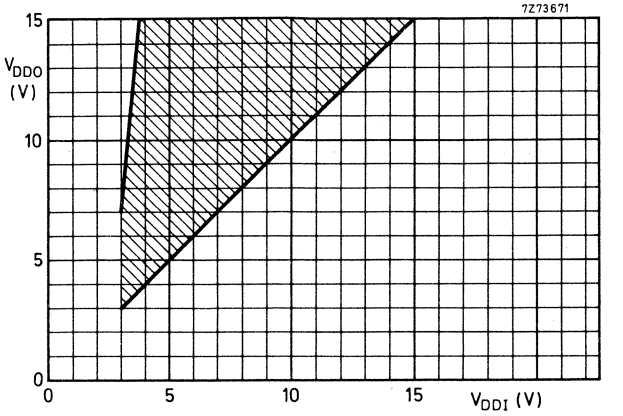


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow Z_n, \overline{Z}_n$	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		65	135	ns	57 ns + (0,16 ns/pF) C_L
	5		170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	80	160	ns	69 ns + (0,23 ns/pF) C_L
	15		70	140	ns	62 ns + (0,16 ns/pF) C_L
Output disable times						
EO $\rightarrow Z_n, \overline{Z}_n$	5		70	135	ns	
HIGH	10	t_{PHZ}	55	110	ns	
	15		60	120	ns	
	5		70	135	ns	
LOW	10	t_{PLZ}	55	105	ns	
	15		55	110	ns	
Output enable times						
EO $\rightarrow Z_n, \overline{Z}_n$	5		195	395	ns	
HIGH	10	t_{PZH}	95	195	ns	
	15		80	165	ns	
	5		195	395	ns	
LOW	10	t_{PZL}	95	190	ns	
	15		80	160	ns	

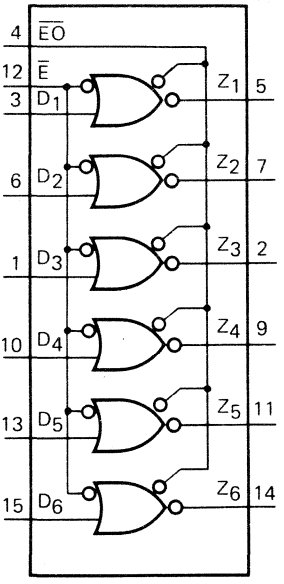
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3 000 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	12 200 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	
	15	31 000 f_i + $\Sigma(f_oC_L) \times V_{DD}^2$	



V_{DDO} as a function of V_{DDI}; the shaded area shows the permissible operating range.

STROBED HEX INVERTER/BUFFER

The HEF4502B consists of six inverter/buffers with 3-state outputs. When the output enable input ($\overline{EO}$) is HIGH all six outputs (Z_1 to Z_6) become high impedance. When the enable input ($\overline{E}$) is HIGH all six outputs are switched to LOW.



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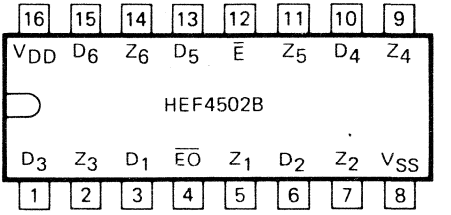

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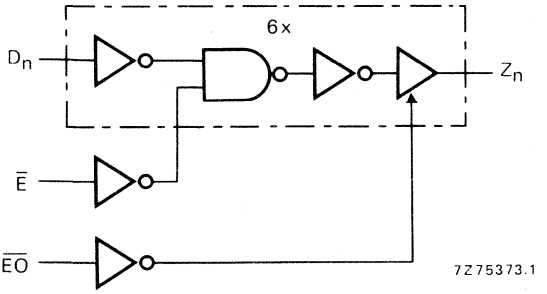
HEF4502BP : 16-lead DIL; plastic (SOT-38Z).
HEF4502BD: 16-lead DIL; ceramic (SOT-74).

LOGIC DIAGRAM



7Z75373.1

PINNING

D_1 to D_6	data inputs
$\overline{E}$	enable input
$\overline{EO}$	output enable input
Z_1 to Z_6	3-state outputs

TRUTH TABLE

D_n	$\overline{E}$	$\overline{EO}$	Z_n
L	L	L	H
H	L	L	L
X	H	L	L
X	X	H	*

* High impedance.

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current HIGH	5	4,6			1,2		1,0		0,8		mA
	10	9,5		$-I_{OH}$	3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
Output current HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4		3,5		2,9		2,3		mA
	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$D_n, \overline{E} \rightarrow Z_n$	5		100	200	ns	90 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	45	90	ns	41 ns + (0,08 ns/pF) C_L
	15		35	65	ns	32 ns + (0,06 ns/pF) C_L
	5		100	200	ns	85 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	45	90	ns	39 ns + (0,13 ns/pF) C_L
	15		35	65	ns	32 ns + (0,05 ns/pF) C_L
Transition times	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
Output disable times						
$\overline{EO} \rightarrow Z_n$	5		45	85	ns	
HIGH	10	t_{PHZ}	35	65	ns	
	15		30	60	ns	
	5		65	135	ns	
LOW	10	t_{PLZ}	40	80	ns	
	15		35	70	ns	
Output enable times						
$\overline{EO} \rightarrow Z_n$	5		70	140	ns	
HIGH	10	t_{PZH}	35	75	ns	
	15		30	65	ns	
	5		90	185	ns	
LOW	10	t_{PZL}	40	85	ns	
	15		35	70	ns	

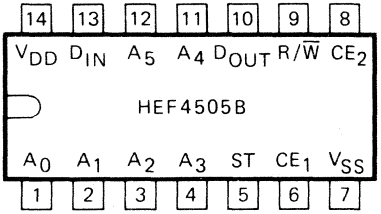
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$5400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = output freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$25\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$96\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

64-BIT, 1-BIT PER WORD RANDOM ACCESS READ/WRITE MEMORY

The HEF4505B is a 64-bit, 1-bit per word, fully decoded and completely static, random access memory. The memory is strobed for reading or writing only when the strobe input (ST), chip enable inputs (CE_1 and CE_2) are HIGH simultaneously. The output data is available at the data output (D_{OUT}) only when the memory is strobed, the read/write input ($R/\overline{W}$) is HIGH and after the read access time has passed. Note that the output is initially disabled and always goes to the LOW state before data is valid. The output is disabled when the memory is not strobed or $R/\overline{W}$ is LOW. $R/\overline{W}$ may remain HIGH during a read cycle or LOW during a write cycle. The output data has the same polarity as the input data.



HEF4505BP : 14-lead DIL; plastic (SOT-27).
HEF4505BD: 14-lead DIL; ceramic (SOT-73).

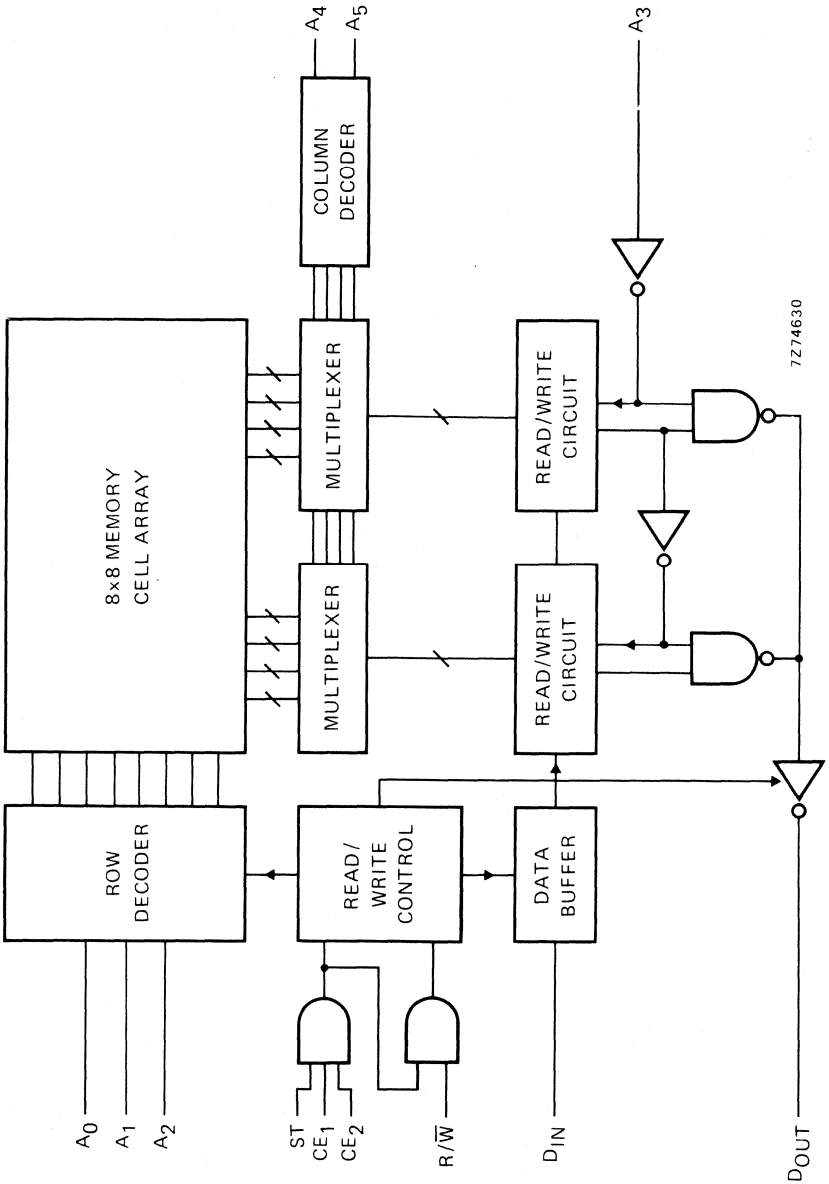
PINNING

A_0 to A_5	address inputs
CE_1, CE_2	chip enable inputs
$R/\overline{W}$	read/write input
ST	strobe input
D_{IN}	data input
D_{OUT}	data output

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 3

BLOCK DIAGRAM



DEVELOPMENT SAMPLE DATA

FUNCTION TABLE

ST, CE_1, CE_2	R/$\overline{W}$	D_{OUT}	mode
L	L	floating	disabled
H	L	floating	write
L	H	floating	disabled
H	H	equal to memory data	read

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Quiescent device current	5	I_{DD}		50		50		375	μA
	10			100		100		750	μA
	15			200		200		1500	μA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

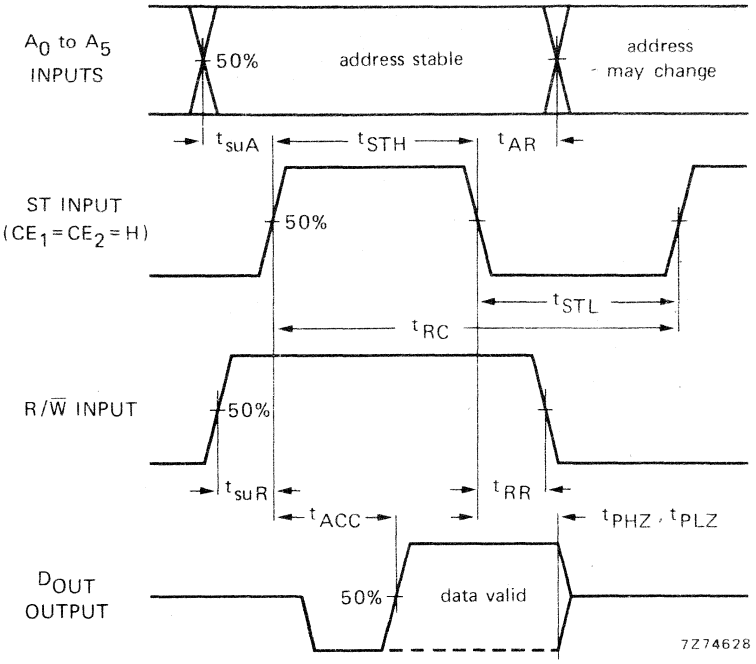
	V_{DD} V	symbol	min	typ	max	
Minimum strobe pulse width; LOW	5	t_{STL}		25		ns
	10			15		ns
	15			10		ns
Read cycle time	5	t_{RC}		350		ns
	10			250		ns
	15			210		ns
Write cycle time	5	t_{WC}		300		ns
	10			220		ns
	15			200		ns
Read access time	5	t_{ACC}		240		ns
	10			100		ns
	15			65		ns
Address recovery time	5	t_{AR}		20		ns
	10			10		ns
	15			5		ns
Read recovery time	5	t_{RR}		−70		ns
	10			−40		ns
	15			−30		ns
Write recovery time	5	t_{WR}		25		ns
	10			15		ns
	15			15		ns

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

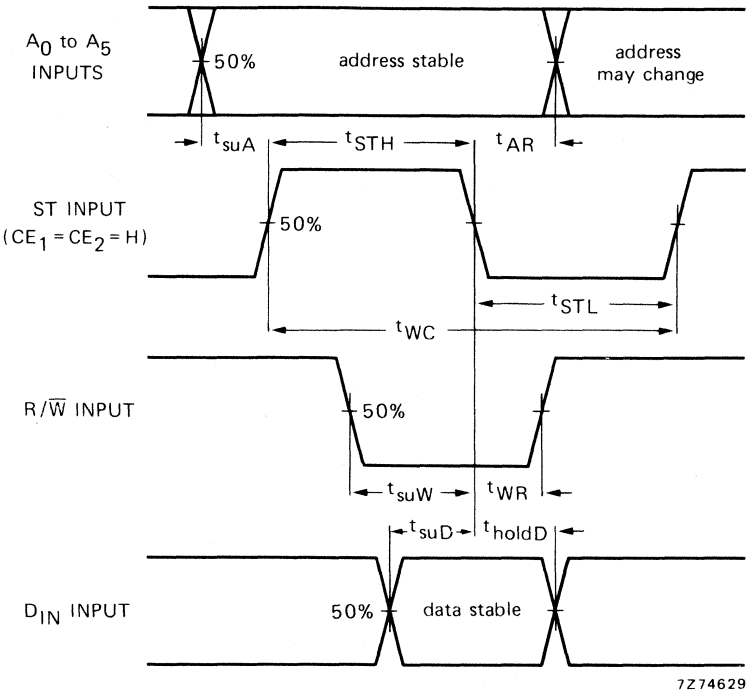
	V_{DD} V	symbol	min	typ	max	
Output disable times	5	t_{PHZ}, t_{PLZ}		75		ns
	10			45		ns
	15			45		ns
Set-up times						
A_n → ST	5	t_{suA}		−70		ns
	10			−35		ns
	15			−25		ns
R/$\overline{W}$ → ST	5	t_{suR}		−100		ns
	10			−50		ns
	15			−35		ns
D_{IN} → ST	5	t_{suD}		50		ns
	10			20		ns
	15			15		ns
R/$\overline{W}$ → ST	5	t_{suW}		80		ns
	10			35		ns
	15			25		ns
Hold time						
D_{IN} → ST	5	t_{holdD}		−40		ns
	10			−10		ns
	15			0		ns

READ CYCLE TIMING DIAGRAM



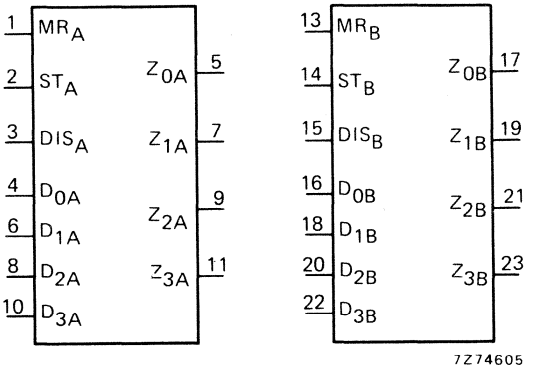
DEVELOPMENT SAMPLE DATA

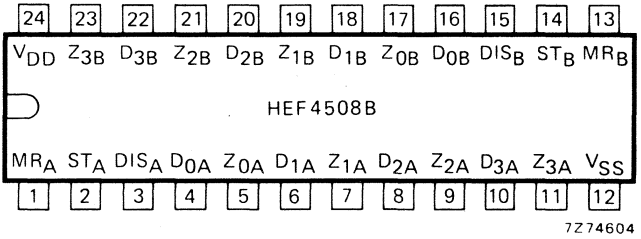
WRITE CYCLE TIMING DIAGRAM



DUAL 4-BIT LATCH

The HEF4508B is a dual 4-bit latch, which consists of two identical, independent 4-bit latches with separate strobe (ST) and master reset (MR) controls. Separate disable inputs (DIS) force the outputs to a high impedance state and allow the device to be used in time-sharing bus line applications.



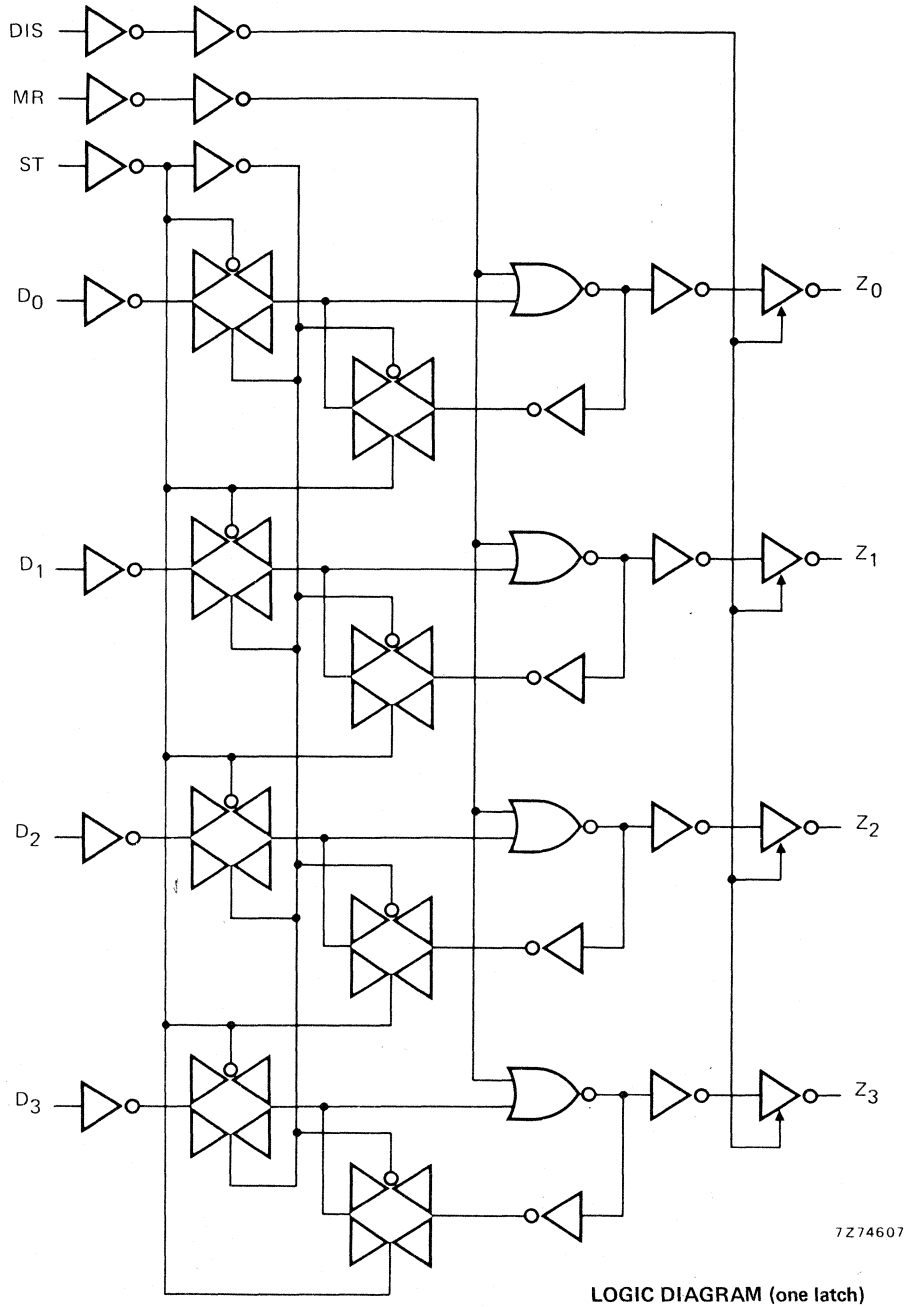


HEF4508BP: 24-lead DIL; plastic (SOT-101A).
HEF4508BD: 24-lead DIL; ceramic (SOT-94).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications



LOGIC DIAGRAM (one latch)

FUNCTION TABLE

inputs				output
MR	ST	DIS	D_n	Z_n
L	H	L	H	H
L	H	L	L	L
L	L	L	X	latched
H	X	L	X	L
X	X	H	X	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance state

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times < 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
ST → Z_n	5			100	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	ns	39 ns + (0,23 ns/pF) C_L
	15			40	ns	32 ns + (0,16 ns/pF) C_L
	5			100	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	ns	39 ns + (0,23 ns/pF) C_L
	15			40	ns	32 ns + (0,16 ns/pF) C_L
Output disable times						
DIS → Z_n	5			60	ns	
HIGH	10	t_{PHZ}		35	ns	
	15			25	ns	
	5			60	ns	
LOW	10	t_{PLZ}		35	ns	
	15			25	ns	
Output enable times						
DIS → Z_n	5			70	ns	
HIGH	10	t_{PZH}		40	ns	
	15			30	ns	
	5			70	ns	
LOW	10	t_{PZL}		40	ns	
	15			30	ns	
Minimum strobe pulse width; HIGH	5			50	ns	
	10	t_{WSTH}		25	ns	
	15			15	ns	
Minimum MR pulse width; HIGH	5			50	ns	
	10	t_{WMRH}		25	ns	
	15			15	ns	
Recovery time for MR	5			0	ns	
	10	t_{RMR}		0	ns	
	15			0	ns	

see also waveforms on page 4

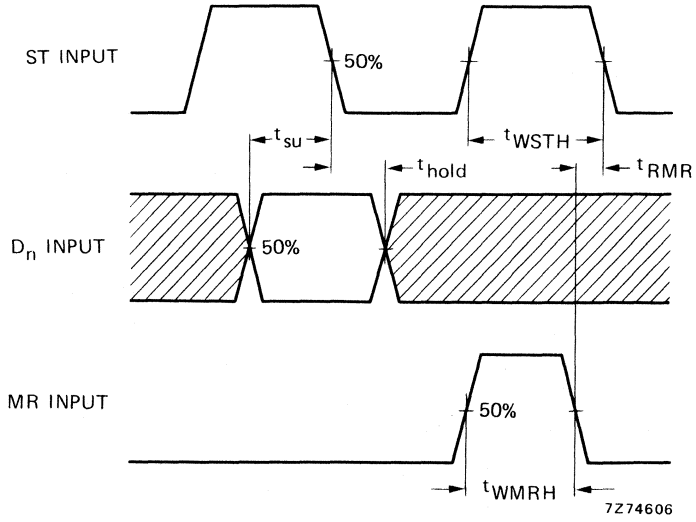
DEVELOPMENT SAMPLE DATA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times < 20 ns

	V_{DD} V	symbol	min	typ	max	
Set-up times						
$D_n \rightarrow$ ST	5			20	ns	see also waveforms below
	10	t_{su}		10	ns	
	15			5	ns	
Hold times						
$D_n \rightarrow$ ST	5			0	ns	
	10	t_{hold}		0	ns	
	15			0	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$8\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

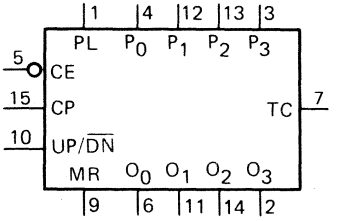


Waveforms showing minimum ST and MR pulse widths, set-up and hold times for D_n to ST and recovery time for MR. Set-up and hold times are shown as positive values but may be specified as negative values.

BCD UP/DOWN COUNTER

The HEF4510B is an edge-triggered synchronous up/down BCD counter with a clock input (CP), an active HIGH up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except the MR input, which must be LOW. With PL LOW, the counter changes on the LOW to HIGH transition of CP if $\overline{CE}$ is LOW. UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when O_0 and O_3 are HIGH and $\overline{CE}$ is LOW. When counting down, TC is LOW when O_0 to O_3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.



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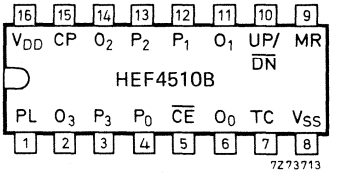

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HEF4510BP: 16-lead DIL; plastic (SOT-38Z).
HEF4510BD: 16-lead DIL; ceramic (SOT-74).

PINNING

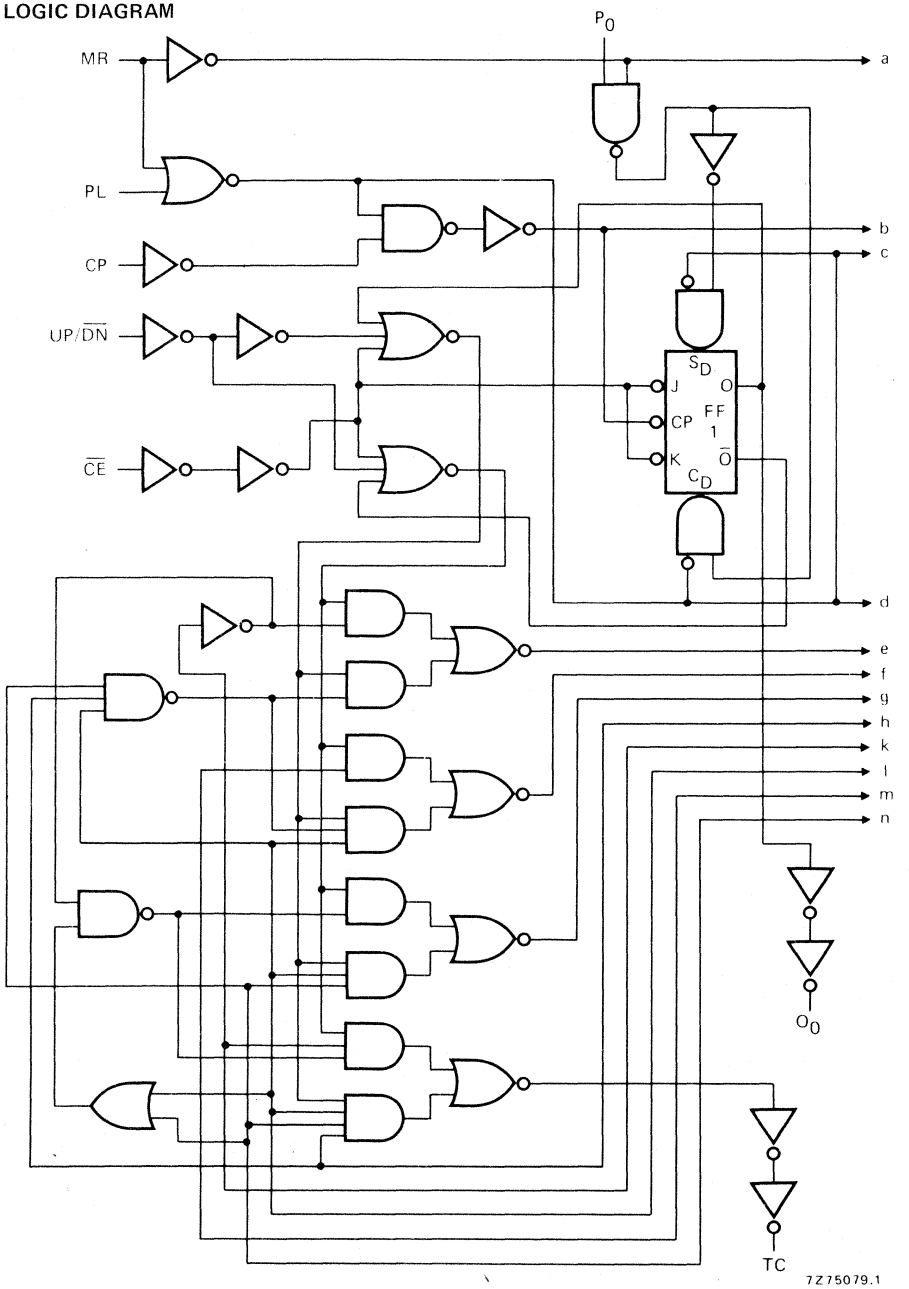
PL	parallel load input (active HIGH)
P_0 to P_3	parallel inputs
$\overline{CE}$	count enable input (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)
UP/$\overline{DN}$	up/down count control input
MR	master reset input
TC	terminal count output (active LOW)
O_0 to O_3	parallel outputs

FAMILY DATA

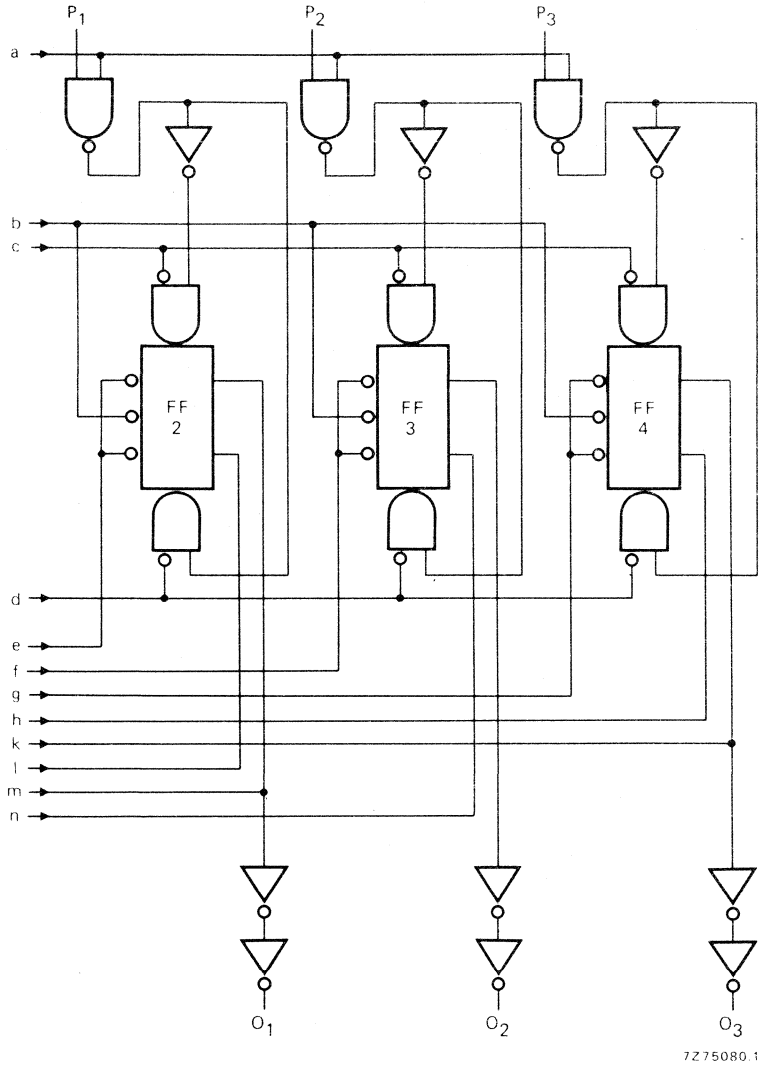
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)

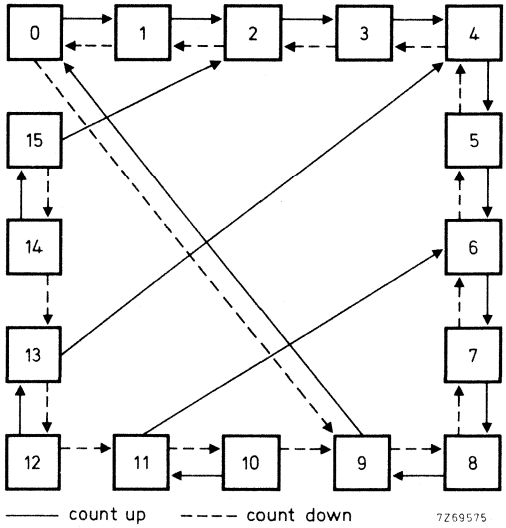


FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	∫	count down
L	L	H	L	∫	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

STATE DIAGRAM



Logic equation for terminal count:

$$TC = \overline{\overline{CE} \cdot \{ (UP/\overline{DN}) \cdot O_0 \cdot O_3 + \overline{(UP/\overline{DN})} \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \}}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1000 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	4500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	11 200 f_i + Σ($f_o C_L$) x V_{DD}^2	

A.C. CHARACTERISTICS

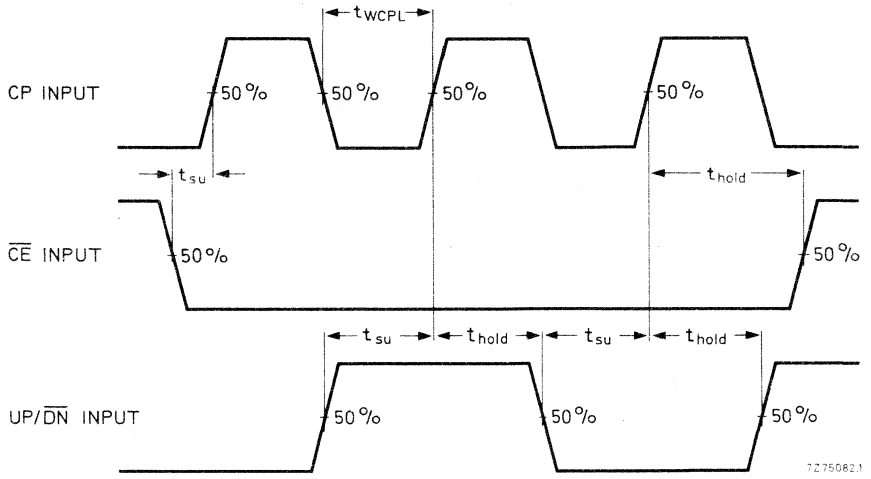
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
CP → TC	5			260	525	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210	ns	94 ns + (0,23 ns/pF) C_L
	15			75	150	ns	67 ns + (0,16 ns/pF) C_L
	5			180	360	ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	115	ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → TC	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135	ns	54 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125	ns	49 ns + (0,23 ns/pF) C_L
	15			45	95	ns	37 ns + (0,16 ns/pF) C_L
MR → O_n, TC	5			205	405	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130	ns	54 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L
MR → TC	5			225	450	ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L

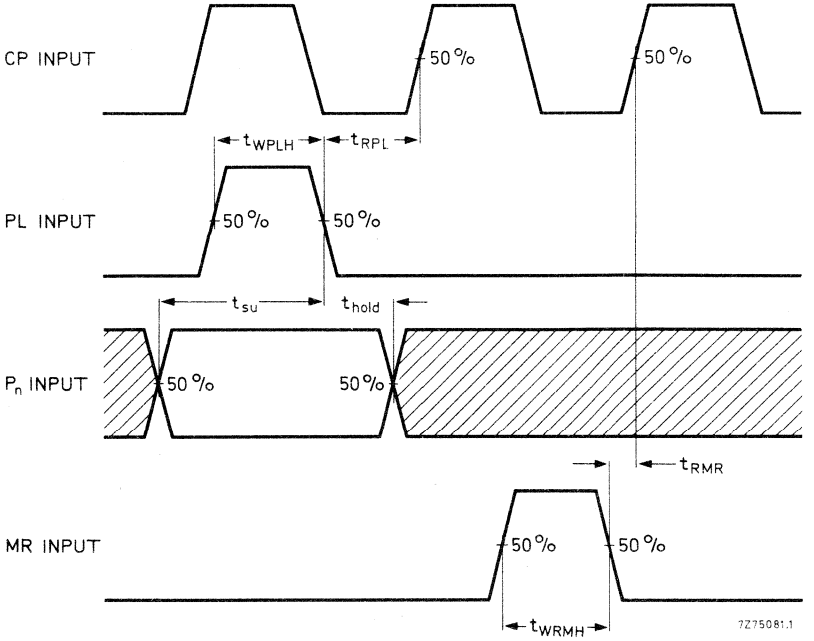
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	95	45		ns	see also waveforms on page 7
	10		35	20		ns	
	15		25	15		ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	105	55		ns	
	10		45	25		ns	
	15		35	15		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	120	60		ns	
	10		50	25		ns	
	15		40	20		ns	
Recovery time for MR	5	t_{RMR}	130	65		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for PL	5	t_{RPL}	150	75		ns	
	10		50	25		ns	
	15		30	15		ns	
Set-up times $P_n \rightarrow PL$	5	t_{su}	100	50		ns	
	10		50	25		ns	
	15		40	20		ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{su}	250	125		ns	
	10		100	50		ns	
	15		75	35		ns	
$\overline{CE} \rightarrow PL$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
Hold times $P_n \rightarrow PL$	5	t_{hold}	10	−40		ns	
	10		5	−20		ns	
	15		0	−20		ns	
$UP/\overline{DN} \rightarrow CP$	5	t_{hold}	35	−90		ns	
	10		15	−35		ns	
	15		15	−25		ns	
$\overline{CE} \rightarrow CP$	5	t_{hold}	20	−40		ns	
	10		5	−15		ns	
	15		5	−10		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	24		MHz	
	15		17	34		MHz	



Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP.

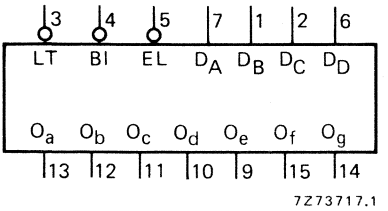


Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4511B is a BCD to 7-segment latch/decoder/driver with four address inputs (D_A to D_D), an active LOW latch enable input ($\overline{EL}$), an active LOW ripple blanking input ($\overline{BI}$), an active LOW lamp test input ($\overline{LT}$), and seven active HIGH n-p-n bipolar segment outputs (O_a to O_g).

When $\overline{EL}$ is LOW, the state of the segment outputs (O_a to O_g) is determined by the data on D_A to D_D. When $\overline{EL}$ goes HIGH, the last data present on D_A to D_D are stored in the latches and the segment outputs remain stable. When $\overline{LT}$ is LOW, all the segment outputs are HIGH independent of all other input conditions. With $\overline{LT}$ HIGH, a LOW on $\overline{BI}$ forces all segment outputs LOW. The inputs $\overline{LT}$ and $\overline{BI}$ do not affect the latch circuit.



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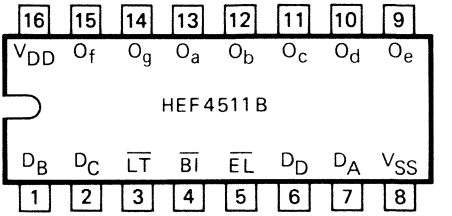


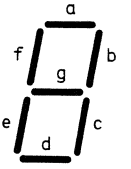
7Z73716.1

HEF4511BP: 16-lead DIL; plastic (SOT-38Z).
HEF4511BD: 16-lead DIL; ceramic (SOT-74).

PINNING

D_A to D_D	address (data) inputs
$\overline{EL}$	latch enable input (active LOW)
$\overline{BI}$	ripple blanking input (active LOW)
$\overline{LT}$	lamp test input (active LOW)
O_a to O_g	segment outputs

SEGMENT DESIGNATION

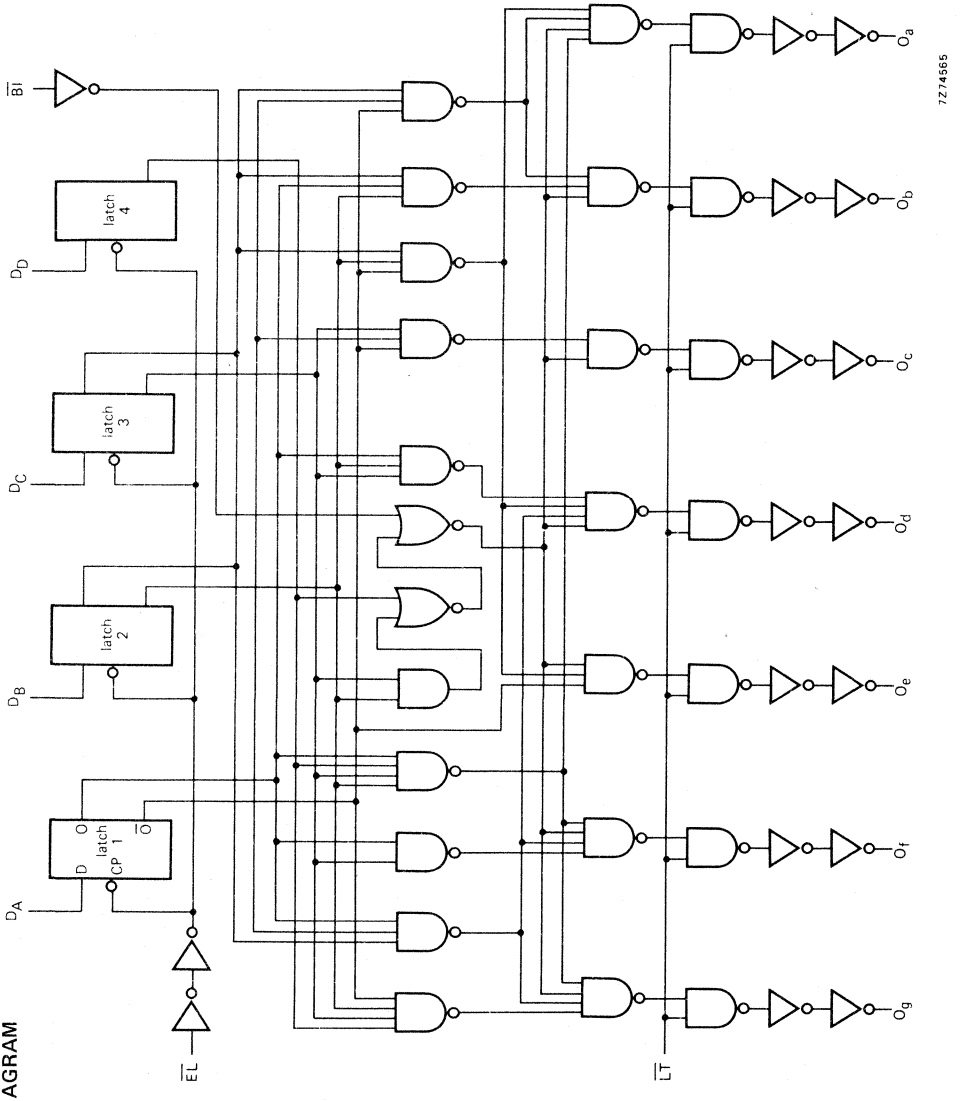


FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



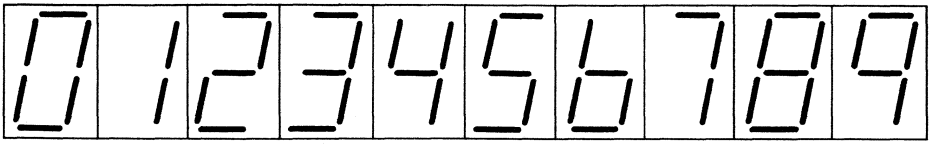
FUNCTION TABLE

inputs							outputs							
$\overline{EL}$	$\overline{BI}$	$\overline{LT}$	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	X	L	X	X	X	X	H	H	H	H	H	H	H	8
X	L	H	X	X	X	X	L	L	L	L	L	L	L	blank
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	L	H	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	L	H	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	L	L	L	L	L	L	L	L	blank
L	H	H	H	H	H	H	L	L	L	L	L	L	L	blank
H	H	H	X	X	X	X				*				*

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* Depends upon the BCD code applied during the LOW to HIGH transition of $\overline{EL}$.

DISPLAY



7Z72856

D.C. CHARACTERISTICS

V_{SS} = 0 V

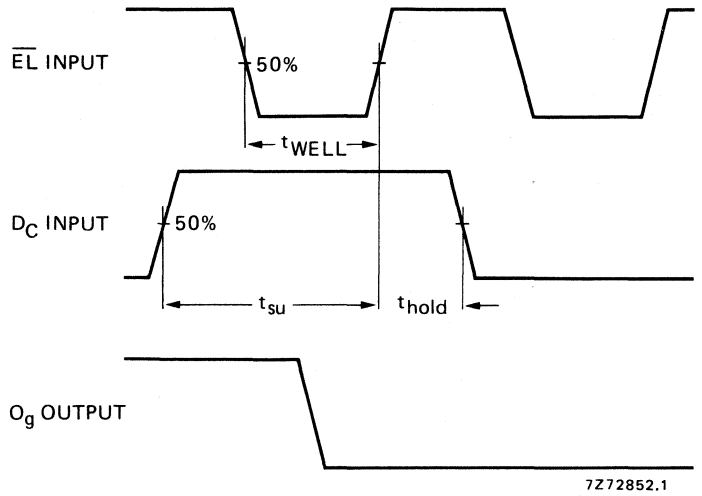
	V_{DD} V	I_{OH} mA	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 typ	+85 min	+85 max	
Output voltage HIGH	5	0	V_{OH}	4,10		4,10	4,40	4,10		V
	10	0		9,10		9,10	9,40	9,10		V
	15	0		14,10		14,10	14,40	14,10		V
Output voltage HIGH	5	5	V_{OH}				4,30			V
	10	5					9,30			V
	15	5					14,30			V
Output voltage HIGH	5	10	V_{OH}	3,60		3,60	4,25	3,30		V
	10	10		8,75		8,75	9,25	8,45		V
	15	10		13,75		13,75	14,25	13,45		V
Output voltage HIGH	5	15	V_{OH}				4,20			V
	10	15					9,20			V
	15	15					14,20			V
Output voltage HIGH	5	20	V_{OH}	2,80		2,80	4,20	2,50		V
	10	20		8,10		8,10	9,20	7,80		V
	15	20		13,10		13,10	14,20	12,80		V
Output voltage HIGH	5	25	V_{OH}				4,15			V
	10	25					9,20			V
	15	25					14,20			V

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
$D_n \rightarrow O_n$	5			155	310 ns	128 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			135	270 ns	108 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
$\overline{EL} \rightarrow O_n$	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5			160	320 ns	133 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
$\overline{BI} \rightarrow O_n$	5			120	240 ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			105	210 ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80 ns	29 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
$\overline{LT} \rightarrow O_n$	5			65	130 ns	38 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		25	50 ns	14 ns + (0,23 ns/pF) C_L
	15			20	40 ns	12 ns + (0,16 ns/pF) C_L
	5			50	100 ns	23 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		25	50 ns	14 ns + (0,23 ns/pF) C_L
	15			20	40 ns	12 ns + (0,16 ns/pF) C_L
Minimum $\overline{EL}$	5		50	25	ns	
pulse width; LOW	10	t_{WELL}	20	10	ns	
	15		16	8	ns	
Set-up time	5		30	15	ns	
$D_n \rightarrow \overline{EL}$	10	t_{su}	10	5	ns	see also waveforms on page 6
	15		10	5	ns	
Hold time	5		25	10	ns	
$D_n \rightarrow \overline{EL}$	10	t_{hold}	10	5	ns	
	15		10	5	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	9 100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	31 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	



Conditions

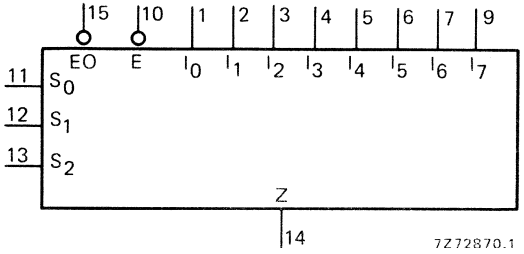
D_D = LOW

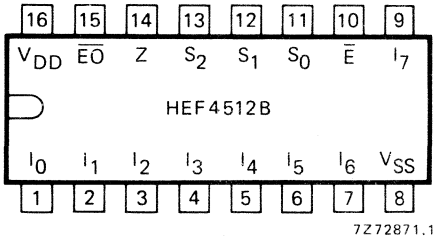
$D_A = D_B = \overline{B_I} = \overline{LT}$ = HIGH

Waveforms showing minimum $\overline{EL}$ pulse width, set-up and hold time for D_C to $\overline{EL}$.

8-INPUT MULTIPLEXER WITH 3-STATE OUTPUT

The HEF4512B is an 8-input multiplexer with active LOW logic and output enables ($\overline{E}$, $\overline{EO}$). One of eight binary inputs is selected by select inputs S_0, S_1 and S_2 and is routed to the output Z. A HIGH on $\overline{EO}$ causes Z to assume a high impedance OFF-state, regardless of other input conditions. This allows the output to interface directly with bus oriented systems (3-state). When the active LOW enable ($\overline{E}$) is HIGH, it forces the output LOW provided $\overline{EO}$ is LOW. By proper manipulation of the inputs, the device can provide any logic functions of four variables. It cannot be used to multiplex analogue signals.





HEF4512BP: 16-lead DIL; plastic (SOT-38Z).
HEF4512BD: 16-lead DIL; ceramic (SOT-74).

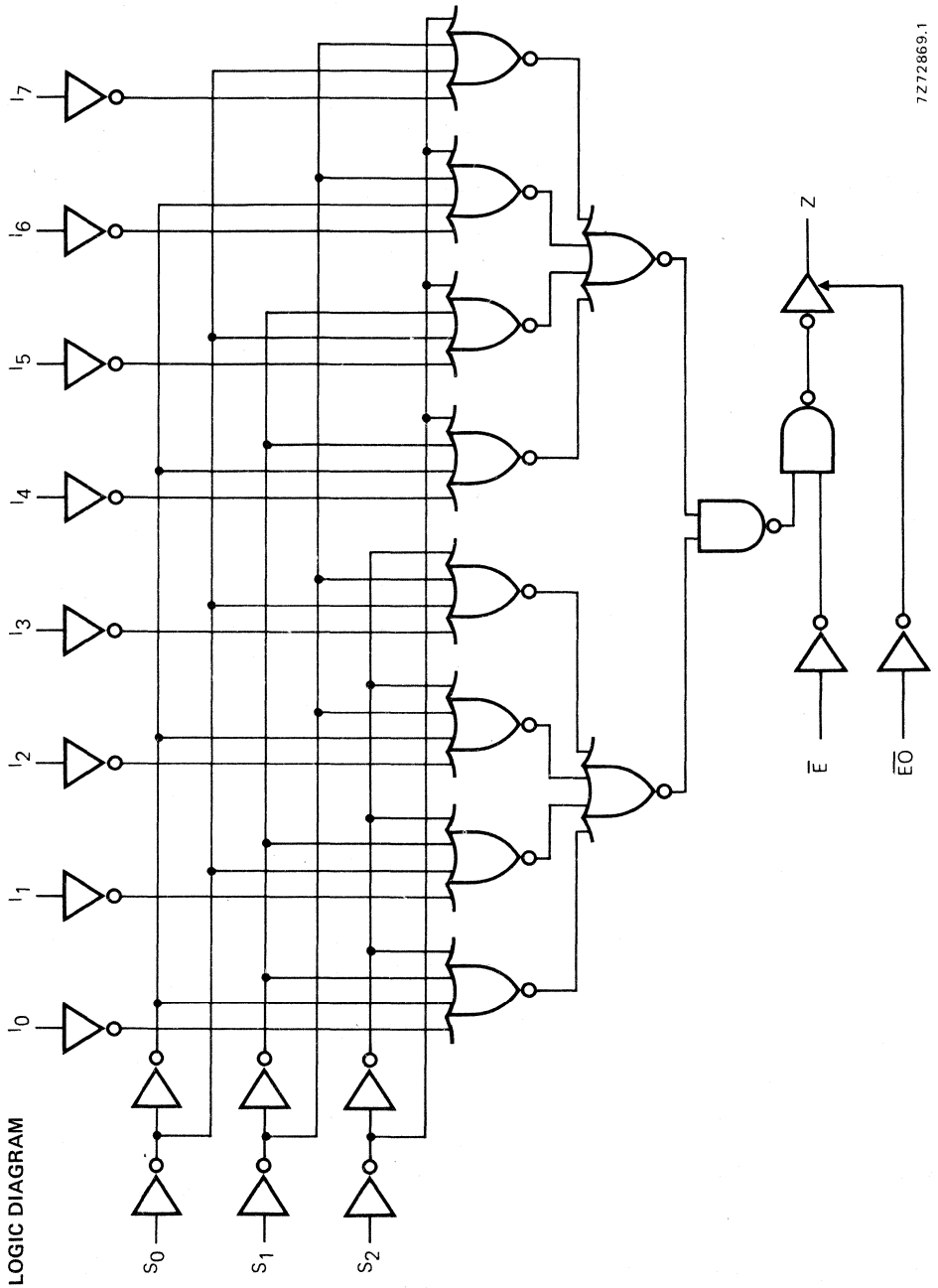
PINNING

S_0, S_1, S_2	select inputs
$\overline{EO}$	output enable (active LOW)
$\overline{E}$	enable (active LOW)
I_0 to I_7	multiplexer inputs
Z	multiplexer output

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

inputs													output
$\overline{EO}$	$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z
L	H	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	L	L	L	X	X	X	X	X	X	X	L
L	L	L	L	L	H	X	X	X	X	X	X	X	H
L	L	L	L	H	X	L	X	X	X	X	X	X	L
L	L	L	L	H	X	H	X	X	X	X	X	X	H
L	L	L	H	L	X	X	L	X	X	X	X	X	L
L	L	L	H	L	X	X	H	X	X	X	X	X	H
L	L	L	H	H	X	X	X	L	X	X	X	X	L
L	L	L	H	H	X	X	X	H	X	X	X	X	H
L	L	H	L	L	X	X	X	X	L	X	X	X	L
L	L	H	L	L	X	X	X	X	H	X	X	X	H
L	L	H	L	H	X	X	X	X	X	L	X	X	L
L	L	H	L	H	X	X	X	X	X	H	X	X	H
L	L	H	H	L	X	X	X	X	X	X	L	X	L
L	L	H	H	L	X	X	X	X	X	X	H	X	H
L	L	H	H	H	X	X	X	X	X	X	X	L	L
L	L	H	H	H	X	X	X	X	X	X	X	H	H
H	X	X	X	X	X	X	X	X	X	X	X	X	Z

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
Z = high impedance OFF-state

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

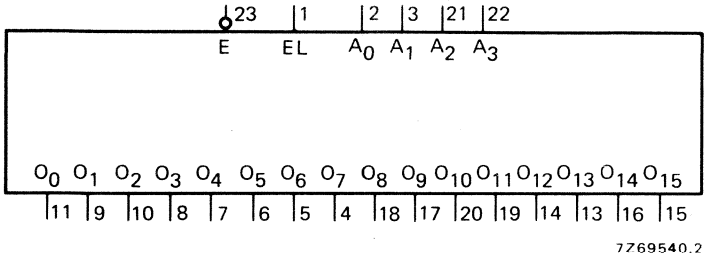
A.C. CHARACTERISTICS

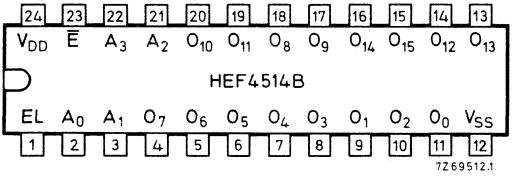
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow Z$	5		100	195	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	24 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
	5		100	205	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	75	ns	29 ns + (0,23 ns/pF) C_L
	15		25	50	ns	17 ns + (0,16 ns/pF) C_L
$S_n \rightarrow Z$	5		140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		35	65	ns	27 ns + (0,16 ns/pF) C_L
	5		140	275	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	50	100	ns	39 ns + (0,23 ns/pF) C_L
	15		35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{E} \rightarrow Z$	5		60	120	ns	33 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	20	45	ns	9 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
	5		55	110	ns	28 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	45	ns	14 ns + (0,23 ns/pF) C_L
	15		15	30	ns	7 ns + (0,16 ns/pF) C_L
Output disable times						
$\overline{EO} \rightarrow Z$	5		20	45	ns	
HIGH	10	t_{PHZ}	10	25	ns	
	15		10	20	ns	
	5		30	60	ns	
LOW	10	t_{PLZ}	15	25	ns	
	15		10	20	ns	
Output enable times						
$\overline{EO} \rightarrow Z$	5		30	55	ns	
HIGH	10	t_{PZH}	10	20	ns	
	15		5	15	ns	
	5		35	70	ns	
LOW	10	t_{PZL}	10	25	ns	
	15		5	15	ns	

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4514B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs (O_0 to O_{15}) are mutually exclusive active HIGH. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is HIGH. At $\overline{E}$ HIGH, all outputs are LOW. The enable input ($\overline{E}$) does not affect the state of the latch.





HEF4514BP : 24-lead DIL; plastic (SOT-101A).
HEF4514BD: 24-lead DIL; ceramic (SOT-94).

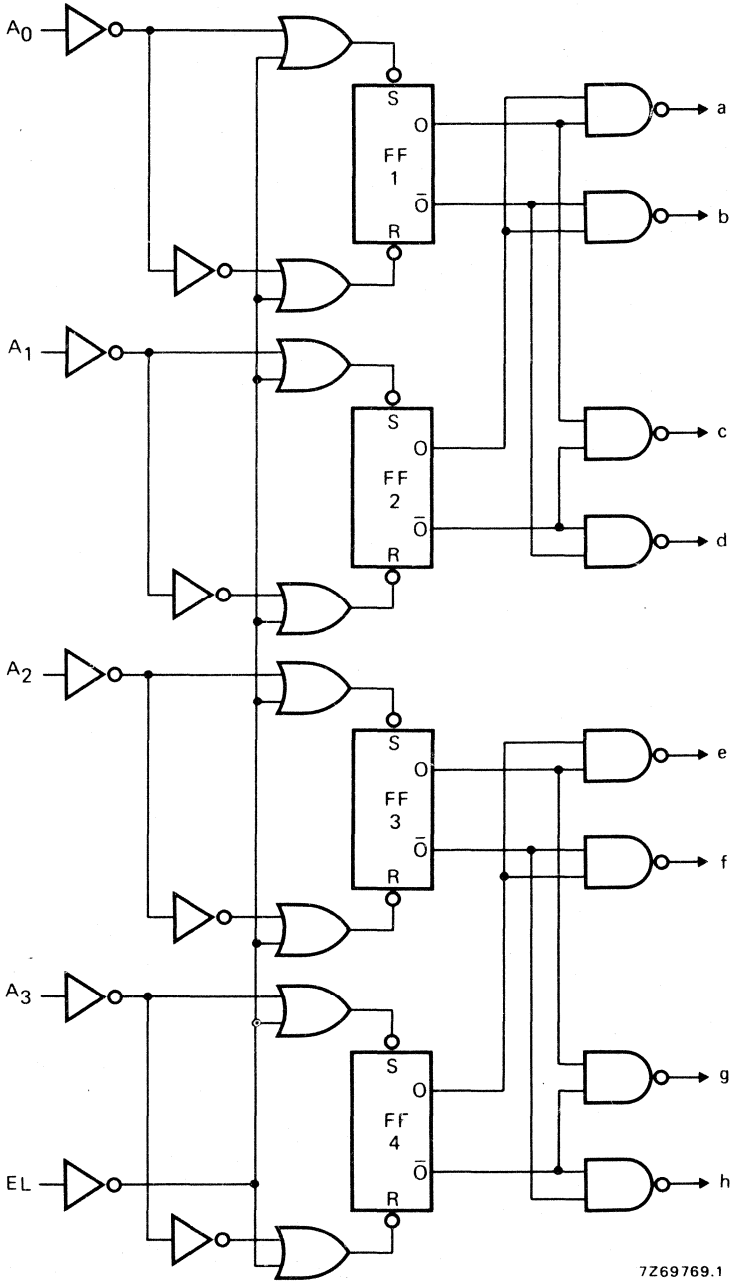
PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active HIGH)

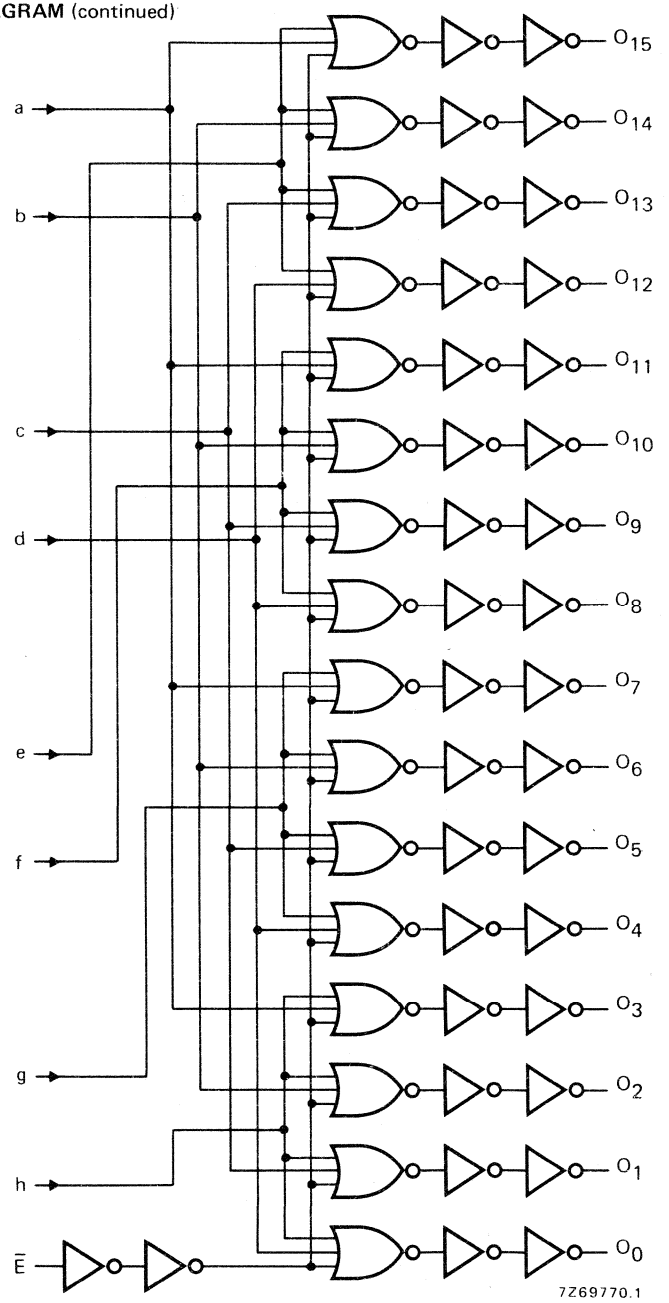
FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



TRUTH TABLE

inputs					outputs														
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
L	L	H	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L
L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L
L	H	H	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L
L	L	L	L	H	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L
L	L	H	L	H	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L
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L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

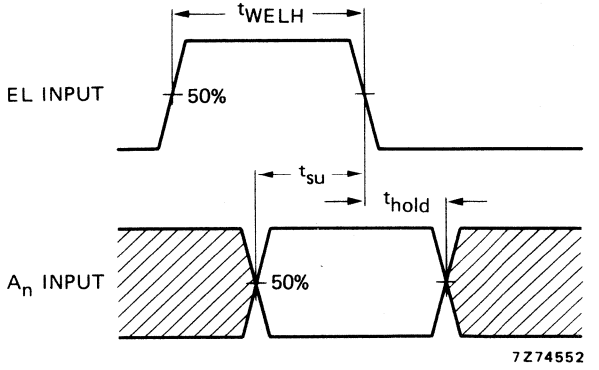
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, EL → O_n	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\overline{E}$ → O_n	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Transition times	5			90	180	ns	40 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		35	65	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
	5			85	170	ns	35 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		35	70	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
Set-up time	5		120	60		ns	see also waveforms below
A_n → EL	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time	5		0	60		ns	
A_n → EL	10	t_{hold}	0	20		ns	
	15		0	15		ns	
Minimum EL pulse	5		120	60		ns	
width; HIGH	10	t_{WELH}	40	20		ns	
	15		30	15		ns	

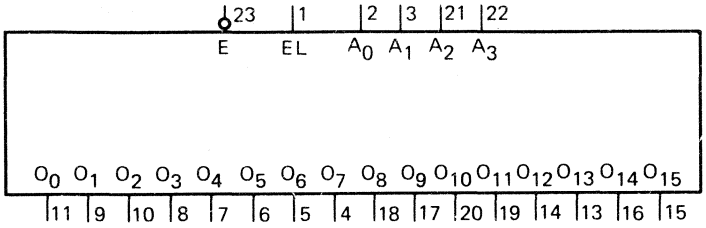
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

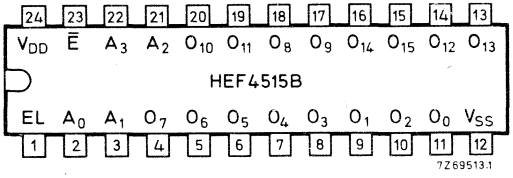


Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as nagative values.

1-OF-16 DECODER/DEMULTIPLEXER WITH INPUT LATCHES

The HEF4515B is a 1-of-16 decoder/demultiplexer, having four binary weighted address inputs (A_0 to A_3), a latch enable input (EL), and an active LOW enable input ($\overline{E}$). The 16 outputs (O_0 to O_{15}) are mutually exclusive active LOW. When EL is HIGH, the selected output is determined by the data on A_n. When EL goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\overline{E}$ is LOW, the selected output, determined by the contents of the latch, is LOW. At $\overline{E}$ HIGH, all outputs are HIGH. The enable input ($\overline{E}$) does not affect the state of the latch.





HEF4515BP : 24-lead DIL; plastic (SOT-101A).
HEF4515BD: 24-lead DIL; ceramic (SOT-94).

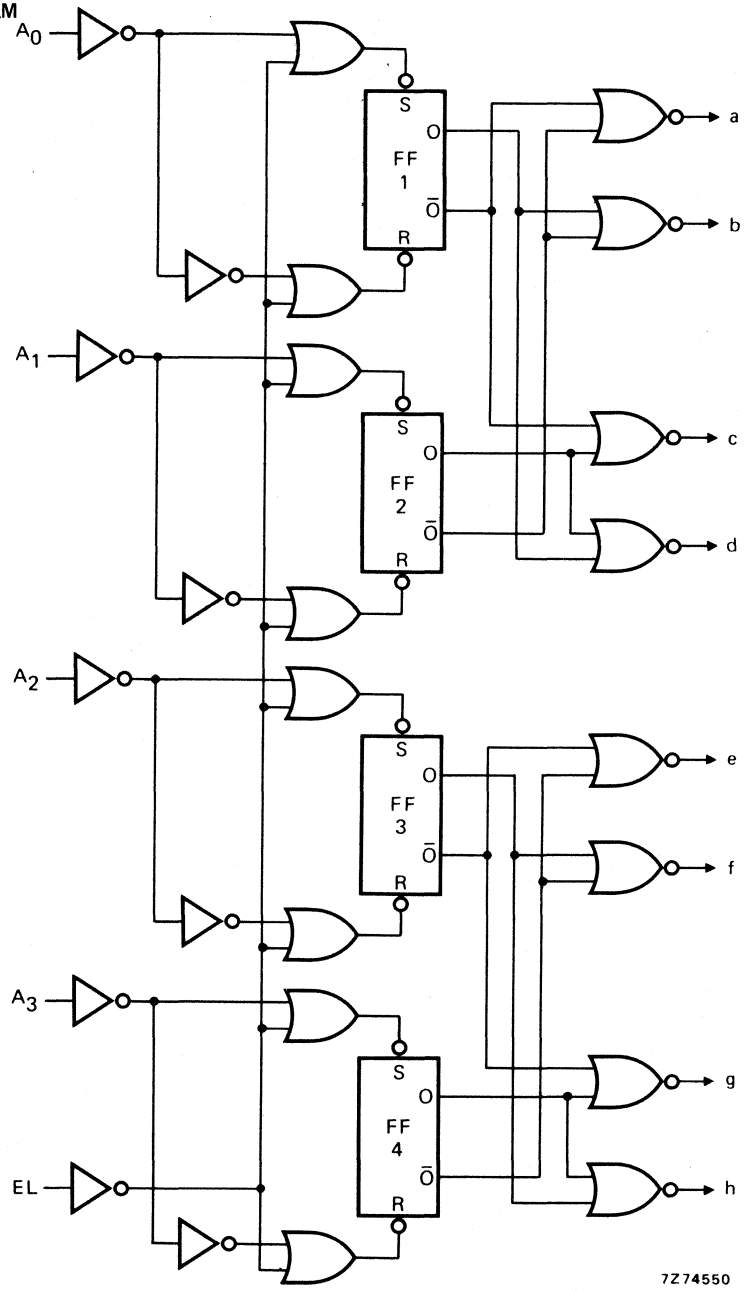
PINNING

A_0 to A_3	address inputs
$\overline{E}$	enable input (active LOW)
EL	latch enable input
O_0 to O_{15}	outputs (active LOW)

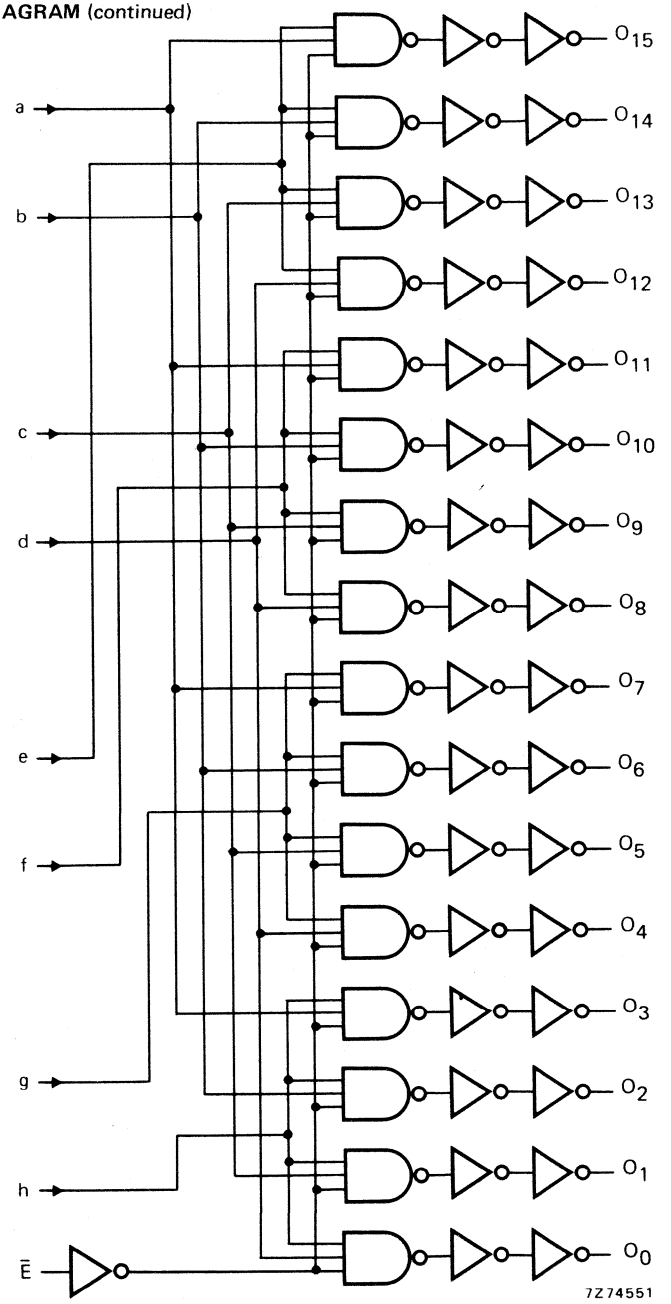
FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



TRUTH TABLE

inputs					outputs													
$\overline{E}$	A_0	A_1	A_2	A_3	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8	O_9	O_{10}	O_{11}	O_{12}	O_{13}	O_{14}	O_{15}
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

EL = HIGH
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

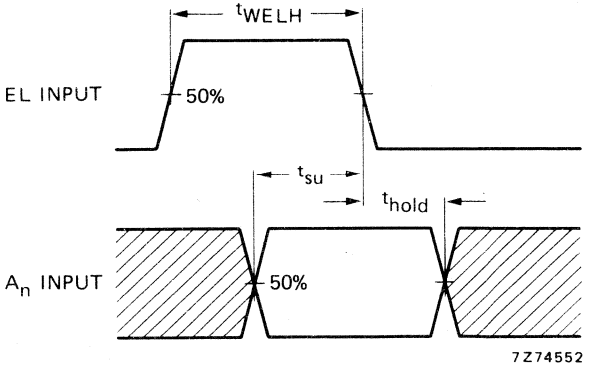
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, EL → O_n	5		260	520	ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
	5		270	550	ns	243 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	95	190	ns	84 ns + (0,23 ns/pF) C_L
	15		65	130	ns	57 ns + (0,16 ns/pF) C_L
$\overline{E}$ → O_n	5		175	350	ns	148 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	65	130	ns	54 ns + (0,23 ns/pF) C_L
	15		45	90	ns	37 ns + (0,16 ns/pF) C_L
	5		200	400	ns	173 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	70	140	ns	59 ns + (0,23 ns/pF) C_L
	15		50	100	ns	42 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Transition times	5			90	180	ns	40 ns + (1,0 ns/pF) C_L
HIGH to LOW	10	t_{THL}		35	65	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
	5			85	170	ns	35 ns + (1,0 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		35	70	ns	14 ns + (0,42 ns/pF) C_L
	15			25	50	ns	11 ns + (0,28 ns/pF) C_L
Set-up time	5		120	60		ns	see also waveforms below
A_n → EL	10	t_{su}	40	20		ns	
	15		30	15		ns	
Hold time	5		0	60		ns	
A_n → EL	10	t_{hold}	0	20		ns	
	15		0	15		ns	
Minimum EL pulse	5		120	60		ns	
width; HIGH	10	t_{WELH}	40	20		ns	
	15		30	15		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1100 f_i + Σ($f_o C_L$) x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5500 f_i + Σ($f_o C_L$) x V_{DD}^2	
	15	16 000 f_i + Σ($f_o C_L$) x V_{DD}^2	

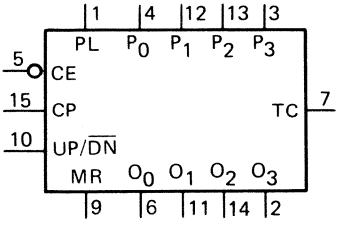


Waveforms showing minimum pulse width for EL, set-up and hold times for A_n to EL. Set-up and hold times are shown as positive values but may be specified as negative values.

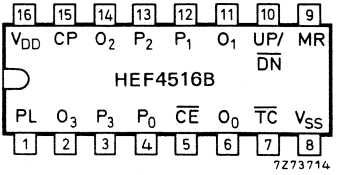
BINARY UP/DOWN COUNTER

The HEF4516B is an edge-triggered synchronous up/down 4-bit binary counter with a clock input (CP), an active HIGH count up/down control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (P_0 to P_3), four parallel outputs (O_0 to O_3), an active LOW terminal count output (TC), and an overriding asynchronous master reset input (MR).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW to HIGH transition of CP. Input UP/$\overline{DN}$ determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, TC is LOW when O_0 to O_3 are HIGH and $\overline{CE}$ is LOW. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of all other input conditions.



7Z73715.1



7Z73714

HEF4516BP: 16-lead DIL; plastic (SOT-38Z).
HEF4516BD: 16-lead DIL; ceramic (SOT-74).

PINNING

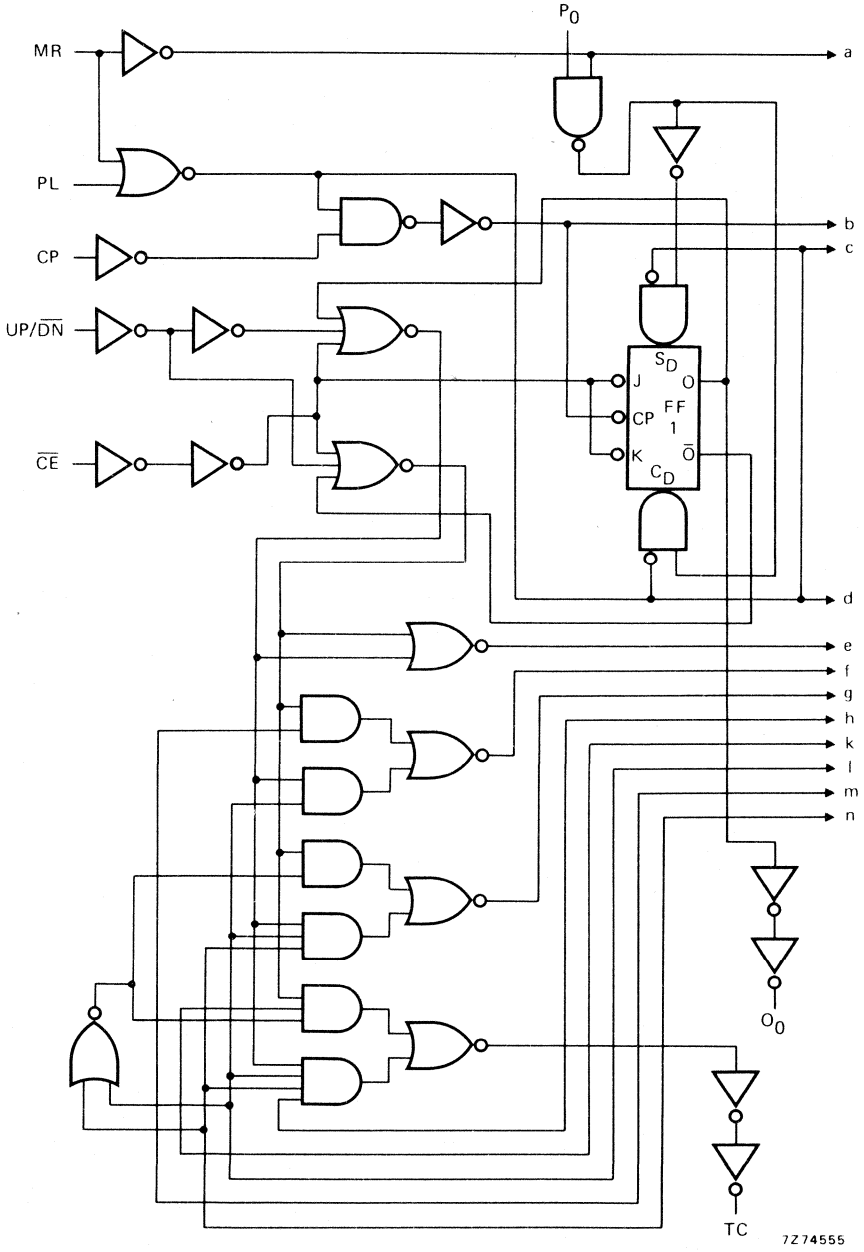
PL	parallel load input (active HIGH)
P_0 to P_3	parallel inputs
$\overline{CE}$	count enable input (active LOW)
CP	clock pulse input (LOW to HIGH, edge triggered)
UP/$\overline{DN}$	up/down count control input
MR	master reset input
TC	terminal count output (active LOW)
O_0 to O_3	parallel outputs

FAMILY DATA

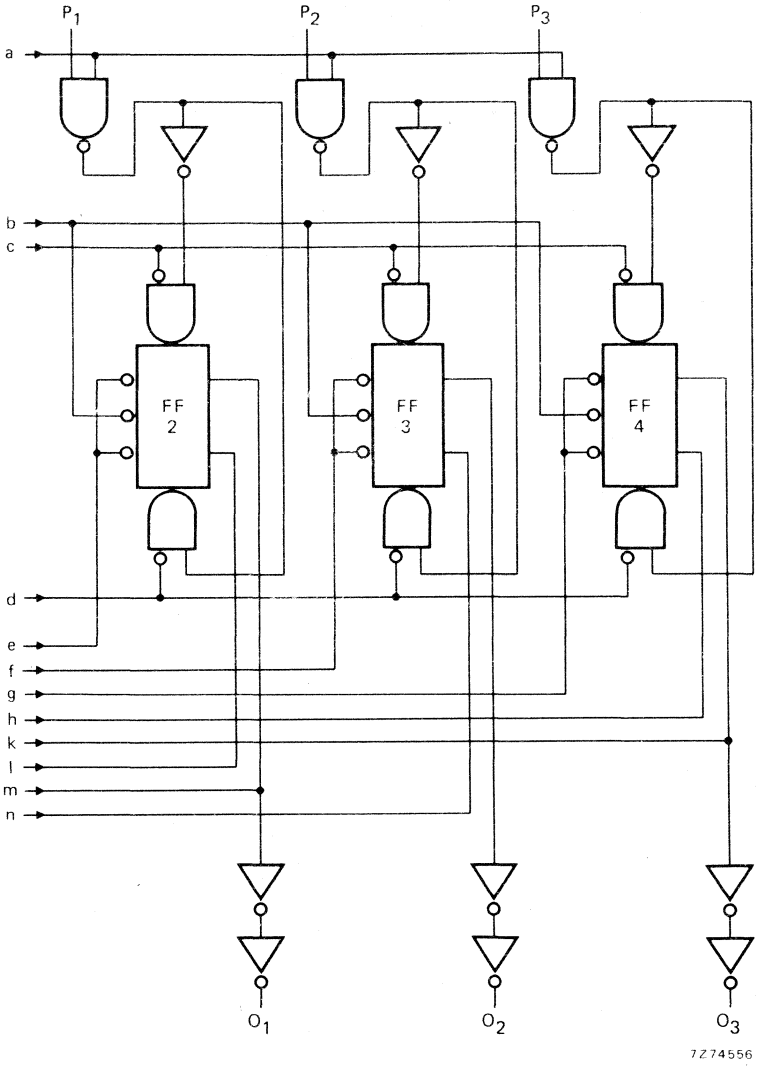
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)

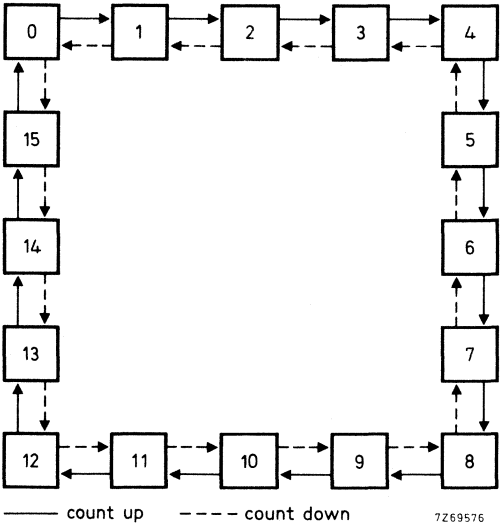


FUNCTION TABLE

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	mode
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	∫	count down
L	L	H	L	∫	count up
H	X	X	X	X	reset

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

STATE DIAGRAM



Logic equation for terminal count:

$$TC = \overline{\overline{CE} \cdot \{(UP/\overline{DN}) \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3 + (\overline{UP/\overline{DN}}) \cdot \overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3\}}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$4500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$11\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

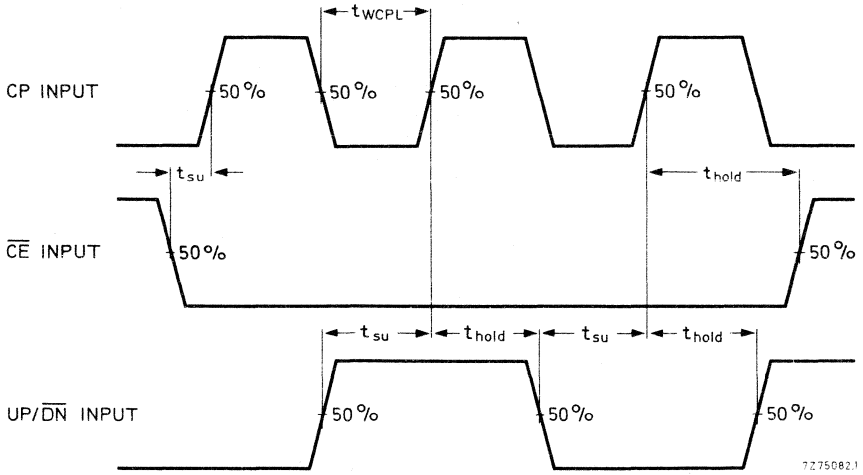
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP → O_n	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
	5			155	310 ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
CP → TC	5			260	525 ns	233 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		105	210 ns	94 ns + (0,23 ns/pF) C_L
	15			75	150 ns	67 ns + (0,16 ns/pF) C_L
	5			180	360 ns	153 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			55	115 ns	47 ns + (0,16 ns/pF) C_L
PL → O_n	5			125	255 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	85 ns	32 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
$\overline{CE}$ → TC	5			165	330 ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	135 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125 ns	49 ns + (0,23 ns/pF) C_L
	15			45	95 ns	37 ns + (0,16 ns/pF) C_L
MR → O_n, TC	5			205	405 ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			45	85 ns	37 ns + (0,16 ns/pF) C_L
MR → TC	5			225	450 ns	198 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L

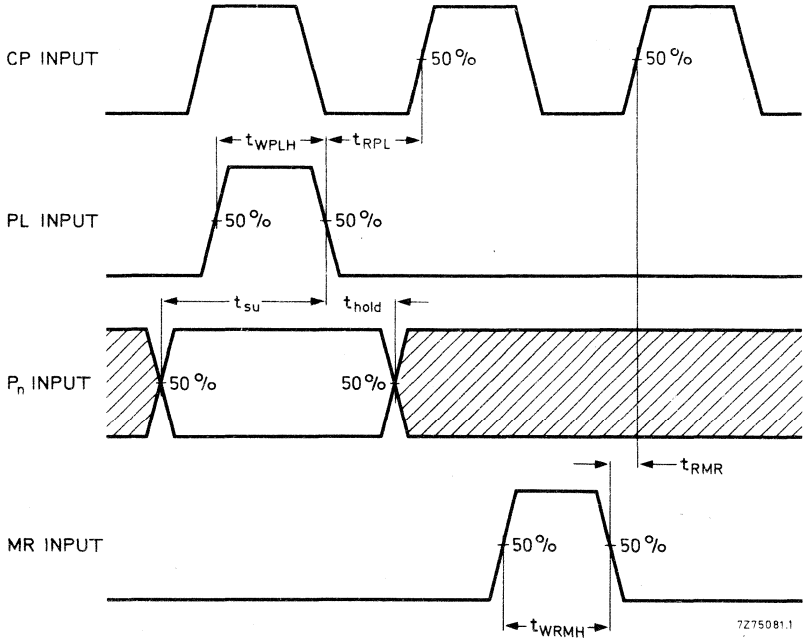
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Minimum clock pulse width; LOW	5	t_{WCPL}	95	45	ns	
	10		35	20	ns	
	15		25	15	ns	
Minimum PL pulse width; HIGH	5	t_{WPLH}	105	55	ns	
	10		45	25	ns	
	15		35	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	120	60	ns	
	10		50	25	ns	
	15		40	20	ns	
Recovery time for MR	5	t_{RMR}	130	65	ns	
	10		45	20	ns	
	15		30	15	ns	
Recovery time for PL	5	t_{RPL}	150	75	ns	
	10		50	25	ns	
	15		30	15	ns	
Set-up times $P_n \longrightarrow PL$	5	t_{su}	100	50	ns	
	10		50	25	ns	
	15		40	20	ns	see also waveforms on page 7
$UP/\overline{DN} \longrightarrow CP$	5	t_{su}	250	125	ns	
	10		100	50	ns	
	15		75	35	ns	
$\overline{CE} \longrightarrow CP$	5	t_{su}	120	60	ns	
	10		40	20	ns	
	15		25	10	ns	
Hold times $P_n \longrightarrow PL$	5	t_{hold}	10	−40	ns	
	10		5	−20	ns	
	15		0	−20	ns	
$UP/\overline{DN} \longrightarrow CP$	5	t_{hold}	35	−90	ns	
	10		15	−35	ns	
	15		15	−25	ns	
$\overline{CE} \longrightarrow CP$	5	t_{hold}	20	−40	ns	
	10		5	−15	ns	
	15		5	−10	ns	
Maximum clock pulse frequency	5	f_{max}	5	10	MHz	
	10		12	24	MHz	
	15		17	34	MHz	



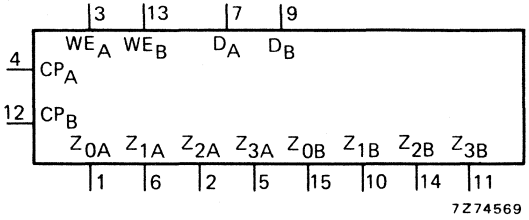
Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP.

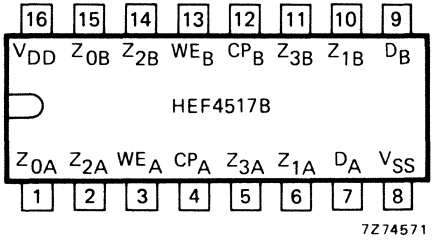


Waveforms showing minimum pulse width for PL and MR, recovery time for PL and MR and set-up and hold times for P_n to PL.

DUAL 64-BIT STATIC SHIFT REGISTER

The HEF4517B consists of two identical, independent 64-bit static shift registers. Each register has separate clock (CP) and write enable (WE) inputs, as well as outputs at bit positions 16, 32, 48 and 64 (Z_0 to Z_3). Data at the data input (D) is entered on the LOW to HIGH transition of the clock, regardless of the state of WE. An output is disabled (high impedance OFF state) when WE is HIGH. During this time, data appearing at D as well as the 16-bit, 32-bit and 48-bit position outputs may be entered into the device by supplying a LOW to HIGH transition of the clock. This feature allows the register to be loaded by 64 bits in 16 clock periods, and also allows usage of bus logic.





HEF4517BP: 16-lead DIL; plastic (SOT-38Z).
HEF4517BD: 16-lead DIL; ceramic (SOT-74).

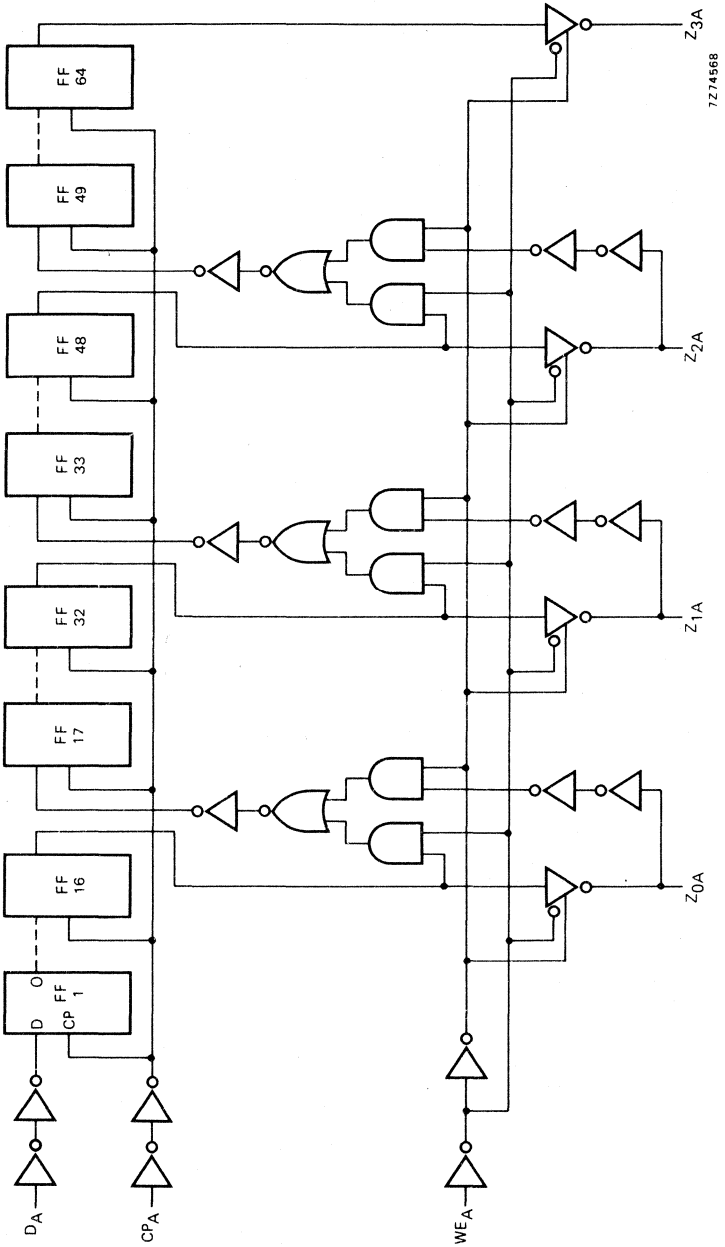
PINNING

CP_A, CP_B	clock inputs
WE_A, WE_B	write enable inputs
D_A, D_B	data inputs
Z_{0A} to Z_{3A}	register outputs
Z_{0B} to Z_{3B}	register outputs

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 4

LOGIC DIAGRAM (one shift register)



FUNCTION TABLE

inputs			outputs			
CP	WE	D	Z_0 (16-bit)	Z_1 (32-bit)	Z_2 (48-bit)	Z_3 (64-bit)
L	L	X	content of 16-bit position displayed	content of 32-bit position displayed	content of 48-bit position displayed	content of 64-bit position displayed
L	H	X	high impedance	high impedance	high impedance	high impedance
H	L	X	content of 16-bit position displayed	content of 32-bit position displayed	content of 48-bit position displayed	content of 64-bit position displayed
H	H	X	high impedance	high impedance	high impedance	high impedance
⎍	L	data entered into 1st bit	content of 16-bit position displayed	content of 32-bit position displayed	content of 48-bit position displayed	content of 64-bit position displayed
⎍	H	data entered into 1st bit	data at Z_0 entered into 17-bit position	data at Z_1 entered into 33-bit position	data at Z_2 entered into 49-bit position	high impedance
⎎	L	X	content of 16-bit position displayed	content of 32-bit position displayed	content of 48-bit position displayed	content of 64-bit position displayed
⎎	H	X	high impedance	high impedance	high impedance	high impedance

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going transition
⎎ = negative-going transition

D.C. CHARACTERISTICS

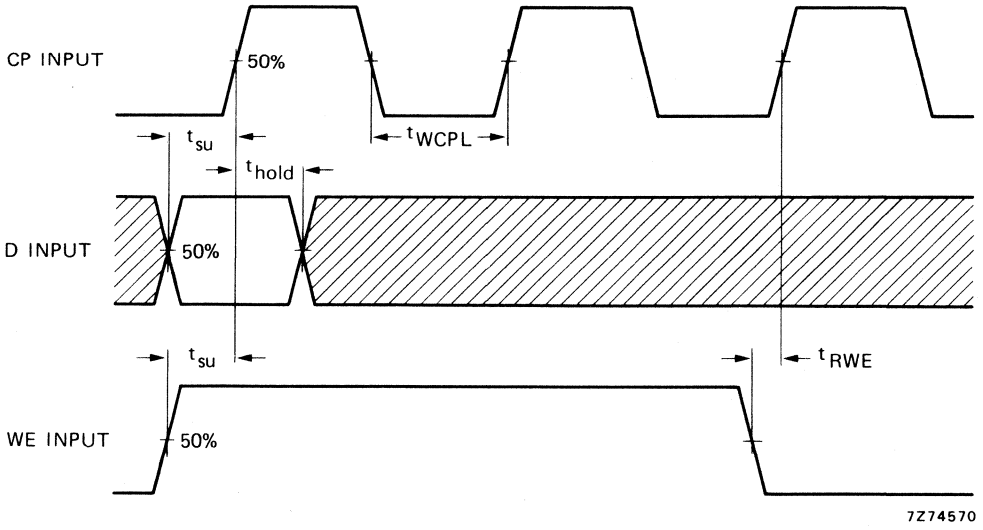
V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Quiesent device current	5	I_{DD}		50		50		375	μA
	10			100		100		750	μA
	15			200		200		1500	μA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$6\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	$25\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	$75\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)



Waveforms showing minimum clock pulse width, set-up and hold times for D to CP, set-up time for WE to CP and recovery time for WE to CP.
Set-up and hold times are shown as positive values but may be specified as negative values.

A.C. CHARACTERISTICS

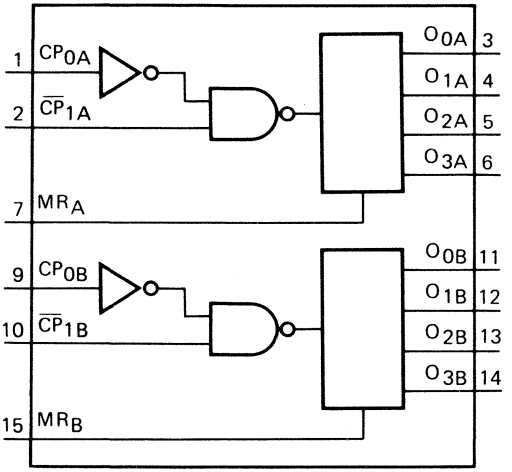
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max	typical extrapolation formula
Propagation delays					
CP → Z_n	5		240	ns	213 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	85	ns	74 ns + (0,23 ns/pF) C_L
	15		60	ns	52 ns + (0,16 ns/pF) C_L
	5		220	ns	193 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	80	ns	69 ns + (0,23 ns/pF) C_L
	15		55	ns	47 ns + (0,16 ns/pF) C_L
Minimum clock pulse width; LOW	5		95	ns	
	10	t_{WCPL}	30	ns	
	15		20	ns	
Set-up times	5		−5	ns	
D → CP	10	t_{su}	0	ns	
	15		0	ns	
	5		100	ns	see also waveforms on page 4
WE → CP	10	t_{su}	50	ns	
	15		30	ns	
Hold time	5		20	ns	
D → CP	10	t_{hold}	10	ns	
	15		5	ns	
Recovery time	5		100	ns	
for WE → CP	10	t_{RWE}	50	ns	
	15		30	ns	
Output disable times					
WE → Z_n	5		45	ns	
HIGH	10	t_{PHZ}	20	ns	
	15		10	ns	
	5		50	ns	
LOW	10	t_{PLZ}	20	ns	
	15		10	ns	
Output enable times					
WE → Z_n	5		25	ns	
HIGH	10	t_{PZH}	15	ns	
	15		10	ns	
	5		40	ns	
LOW	10	t_{PZL}	20	ns	
	15		15	ns	
Maximum clock pulse frequency	5		5	MHz	
	10	f_{max}	14	MHz	
	15		20	MHz	

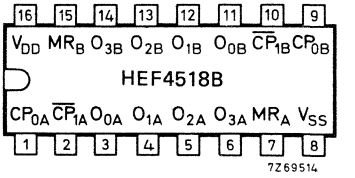
DEVELOPMENT SAMPLE DATA

DUAL BCD COUNTER

The HEF4518B is a dual 4-bit internally synchronous BCD counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input ($\overline{CP}_1$), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if $\overline{CP}_1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}_1$ input if CP_0 is LOW. Either CP_0 or $\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of CP_0, $\overline{CP}_1$.



7Z69556.1



7Z69514

HEF4518BP: 16-lead DIL; plastic (SOT-38Z).
HEF4518BD: 16-lead DIL; ceramic (SOT-74).

PINNING

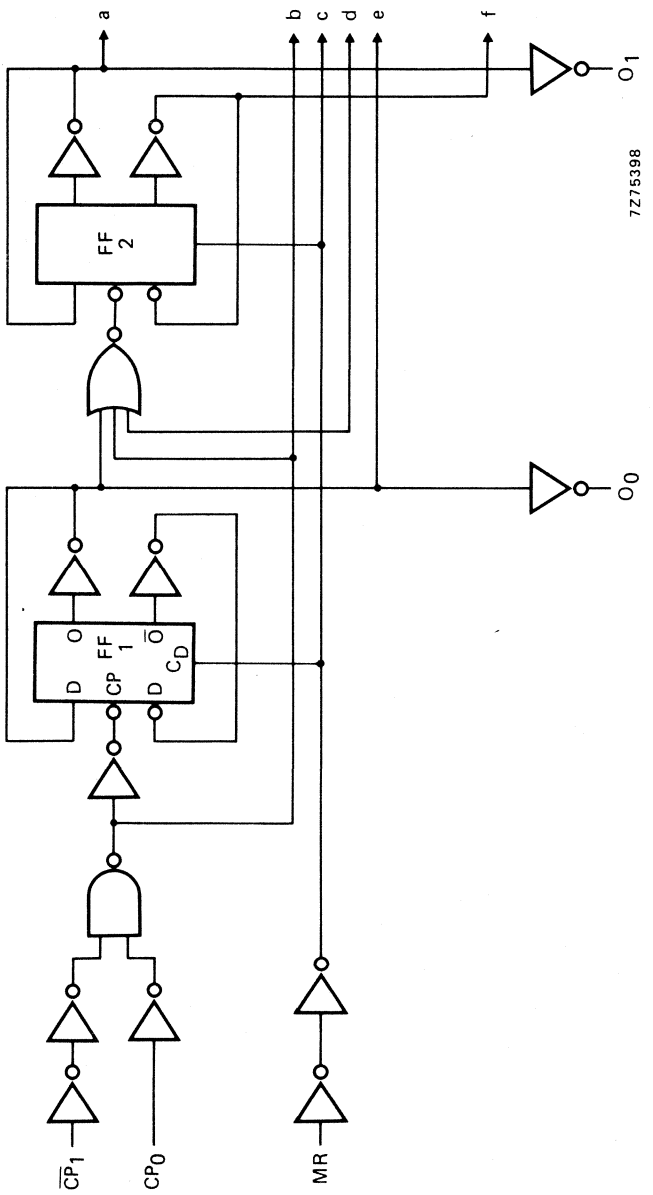
CP_{0A}, CP_{0B}	clock inputs (L to H triggered)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$	clock inputs (H to L triggered)
MR_A, MR_B	master reset inputs
O_{0A} to O_{3A}	outputs
O_{0B} to O_{3B}	outputs

FAMILY DATA

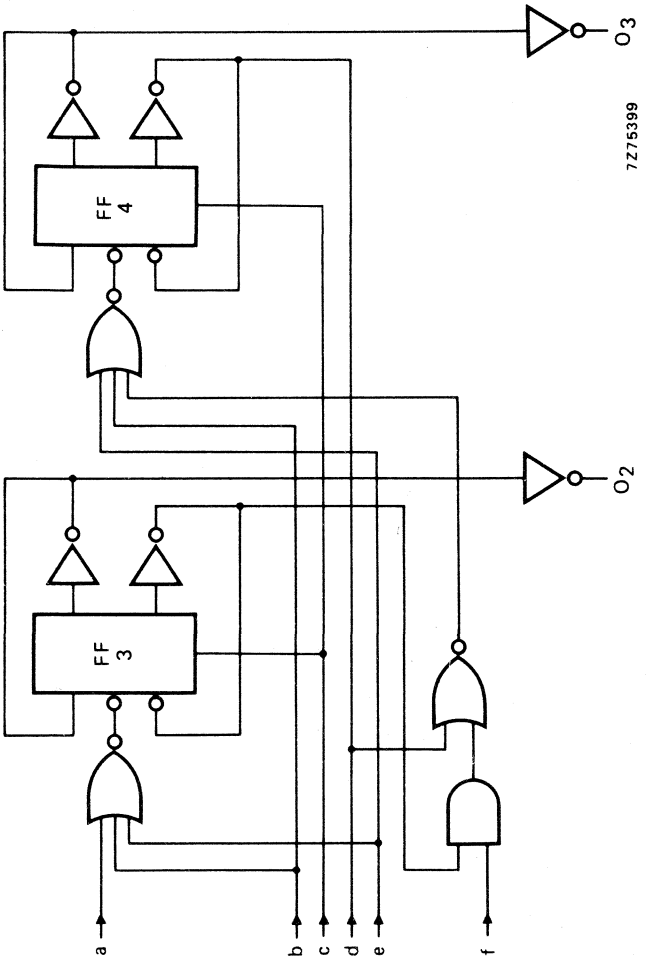
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM (one counter)



LOGIC DIAGRAM (continued)



FUNCTION TABLE

CP_0	$\overline{CP}_1$	MR	mode
∫	H	L	counter advances
L	⌝	L	counter advances
⌝	X	L	no change
X	∫	L	no change
∫	L	L	no change
H	⌝	L	no change
X	X	H	O_0 to O_3 = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌝ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

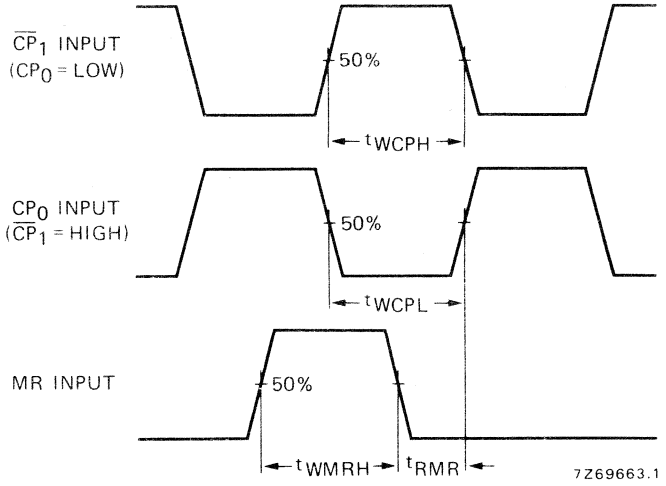
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP_0, $\overline{CP}_1$ → O_n	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145 ns	64 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
Minimum CP_0	5		165	85	ns	
pulse width; LOW	10	t_{WCPL}	65	30	ns	
	15		45	25	ns	
Minimum $\overline{CP}_1$	5		165	85	ns	
pulse width; HIGH	10	t_{WCPH}	65	30	ns	
	15		45	25	ns	
Minimum MR	5		90	45	ns	
pulse width; HIGH	10	t_{WMRH}	40	20	ns	
	15		30	15	ns	
Recovery time	5		25	10	ns	
for MR	10	t_{RMR}	15	5	ns	
	15		10	5	ns	
Set-up times	5		180	90	ns	
CP_0 → $\overline{CP}_1$	10	t_{su}	70	35	ns	
	15		50	25	ns	
	5		150	75	ns	
$\overline{CP}_1$ → CP_0	10	t_{su}	60	30	ns	
	15		40	20	ns	
Maximum clock	5		3	6	MHz	
pulse frequency	10	f_{max}	7	15	MHz	
	15		10	21	MHz	

see also waveforms on page 5

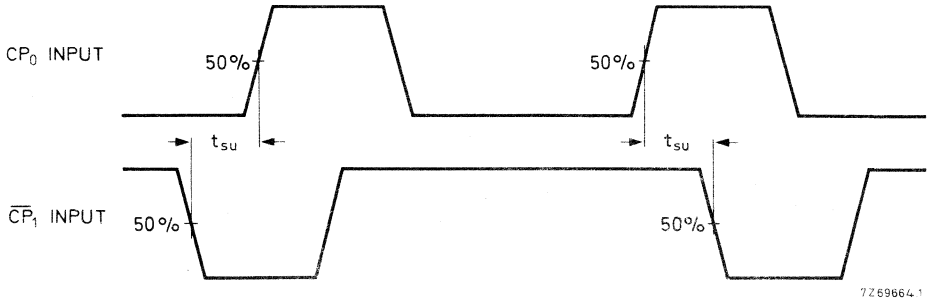
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$750\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths.



Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0. Set-up times are shown as positive values but may be specified as negative values.

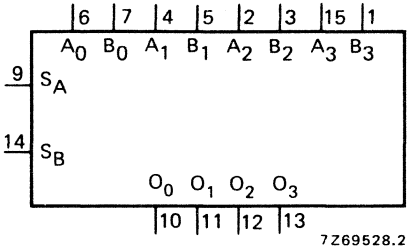
QUADRUPLE 2-INPUT MULTIPLEXER

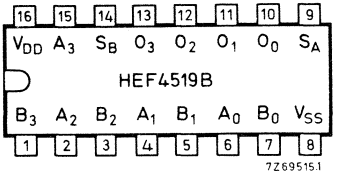
The HEF4519B provides four multiplexing circuits with common select inputs; each circuit contains two inputs and one output. It may be used to select four bits of information from one of two sources.

The 'A' inputs are selected when S_A is HIGH, the 'B' inputs when S_B is HIGH. When S_A and S_B are HIGH, the output (O_n) is the logical EXCLUSIVE-NOR of the A_n and B_n inputs ($O_n = A_n \odot B_n$).

When S_A and S_B are LOW, the output (O_n) is LOW, independent of the multiplexer inputs (A_n and B_n).

The HEF4519B cannot be used to multiplex analogue signals. The outputs utilize standard buffers for best performance.

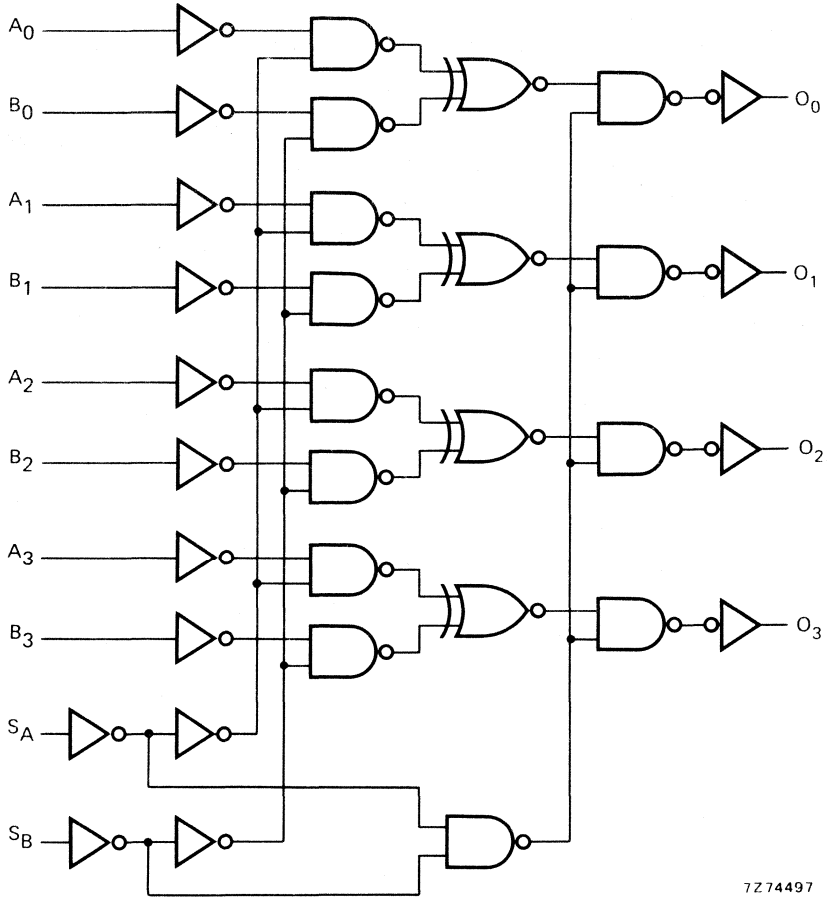




HEF4519BP: 16-lead DIL; plastic (SOT-38Z).
HEF4519BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA
I_{DD} LIMITS category MSI
} see Family Specifications

LOGIC DIAGRAM



PINNING

S_A, S_B	select inputs (active HIGH)
A_0 to A_3	multiplexer inputs
B_0 to B_3	multiplexer inputs
O_0 to O_3	multiplexer outputs

TRUTH TABLE

inputs				output
S_A	S_B	A_n	B_n	O_n
L	L	X	X	L
H	L	A_n	X	A_n
L	H	X	B_n	B_n
H	H	L	L	H
H	H	H	L	L
H	H	L	H	L
H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

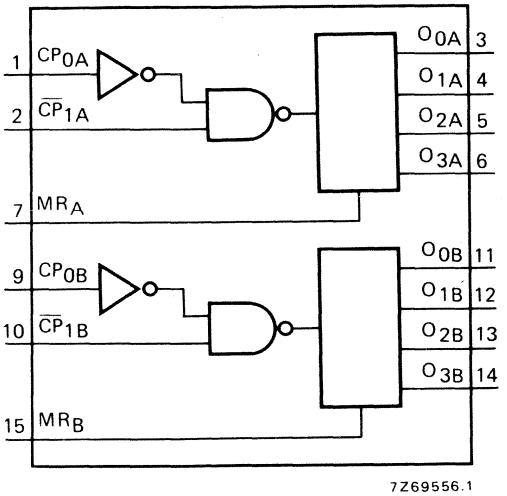
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5		100	200	ns	73 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	45	90	ns	34 ns + (0,23 ns/pF)C_L
	15		35	65	ns	27 ns + (0,16 ns/pF)C_L
	5		90	180	ns	63 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	60	ns	22 ns + (0,16 ns/pF)C_L
S_A, S_B → O_n	5		95	190	ns	68 ns + (0,55 ns/pF)C_L
HIGH to LOW	10	t_{PHL}	40	80	ns	29 ns + (0,23 ns/pF)C_L
	15		30	55	ns	22 ns + (0,16 ns/pF)C_L
	5		85	165	ns	58 ns + (0,55 ns/pF)C_L
LOW to HIGH	10	t_{PLH}	40	75	ns	29 ns + (0,23 ns/pF)C_L
	15		30	55	ns	22 ns + (0,16 ns/pF)C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1400 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	6000 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	
	15	17 100 f_i + $\Sigma(f_oC_L)$ × V_{DD}^2	

DUAL BINARY COUNTER

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (CP_0) and an active LOW clock input ($\overline{CP}_1$), buffered outputs from all four bit positions (O_0 to O_3) and an active HIGH overriding asynchronous master reset input (MR). The counter advances on either the LOW to HIGH transition of the CP_0 input if $\overline{CP}_1$ is HIGH or the HIGH to LOW transition of the $\overline{CP}_1$ input if CP_0 is LOW. Either CP_0 or $\overline{CP}_1$ may be used as the clock input to the counter and the other clock input may be used as a clock enable input. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of CP_0, $\overline{CP}_1$.



HEF4520BP : 16-lead DIL; plastic (SOT-38Z).
HEF4520BD: 16-lead DIL; ceramic (SOT-74).

PINNING

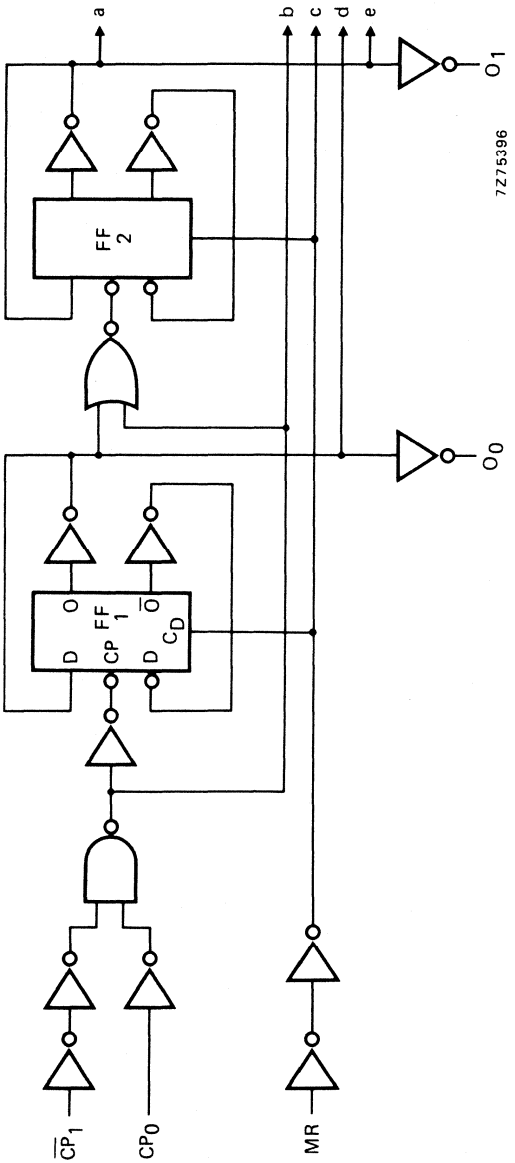
CP_{0A}, CP_{0B}	clock inputs (L to H triggered)
$\overline{CP}_{1A}$, $\overline{CP}_{1B}$	clock inputs (H to L triggered)
MR_A, MR_B	master reset inputs
O_{0A} to O_{3A}	outputs
O_{0B} to O_{3B}	outputs

FAMILY DATA

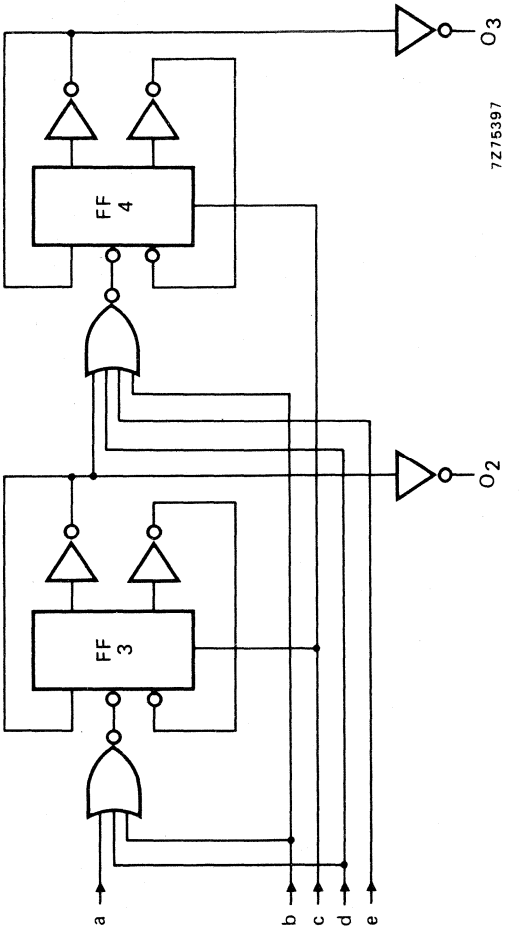
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM (one counter)



LOGIC DIAGRAM (continued)



FUNCTION TABLE

CP_0	$\overline{CP}_1$	MR	mode
∫	H	L	counter advances
L	⤵	L	counter advances
⤵	X	L	no change
X	∫	L	no change
∫	L	L	no change
H	⤵	L	no change
X	X	H	O_0 to O_3 = LOW

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⤵ = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

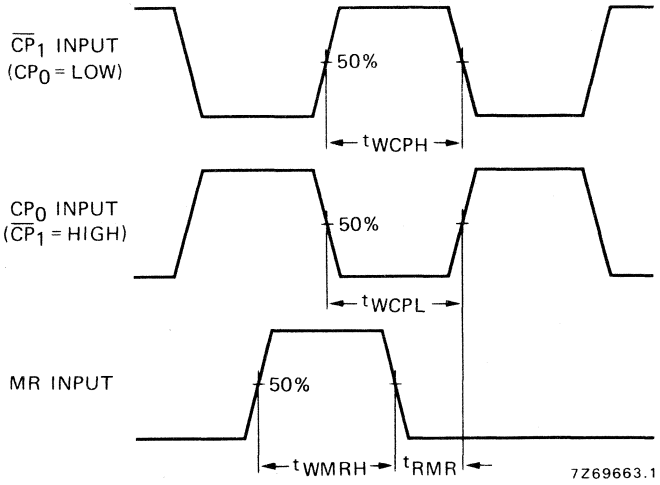
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP_0, $\overline{CP}_1$ → O_n	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	145 ns	64 ns + (0,23 ns/pF) C_L
	15			50	105 ns	42 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		65	130 ns	54 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
MR → O_n	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
Minimum CP_0	5		165	85	ns	
pulse width; LOW	10	t_{WCPL}	65	30	ns	
	15		45	25	ns	
Minimum $\overline{CP}_1$	5		165	85	ns	
pulse width; HIGH	10	t_{WCPH}	65	30	ns	
	15		45	25	ns	
Minimum MR	5		90	45	ns	
pulse width; HIGH	10	t_{WMRH}	40	20	ns	
	15		30	15	ns	
Recovery time	5		25	10	ns	
for MR	10	t_{RMR}	15	5	ns	
	15		10	5	ns	
Set-up times	5		180	90	ns	
CP_0 → $\overline{CP}_1$	10	t_{su}	70	35	ns	
	15		50	25	ns	
	5		150	75	ns	
$\overline{CP}_1$ → CP_0	10	t_{su}	60	30	ns	
	15		40	20	ns	
Maximum clock	5		3	6	MHz	
pulse frequency	10	f_{max}	7	15	MHz	
	15		10	21	MHz	

see also waveforms on page 5

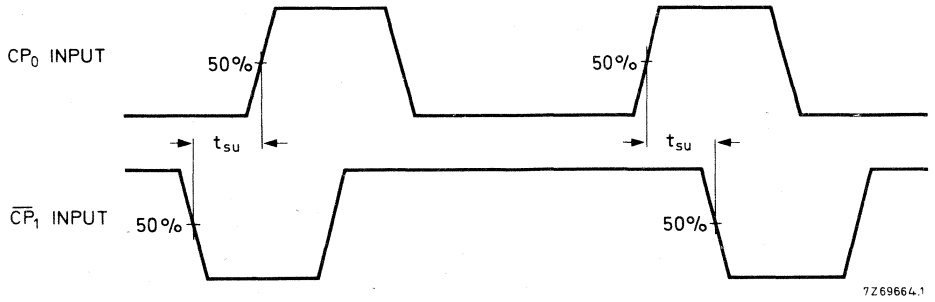
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$750\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$8100\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



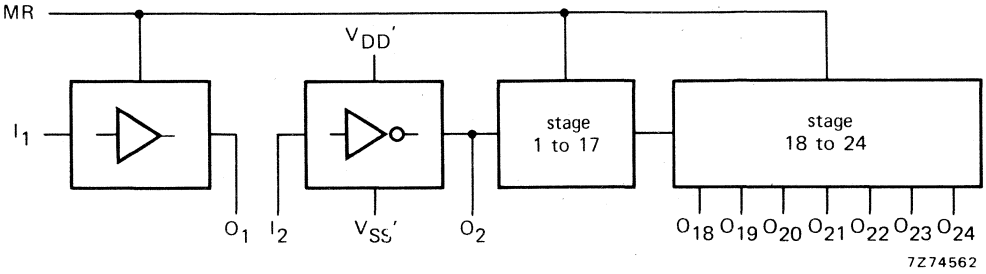
Waveforms showing recovery time for MR; minimum CP_0, $\overline{CP}_1$ and MR pulse widths.

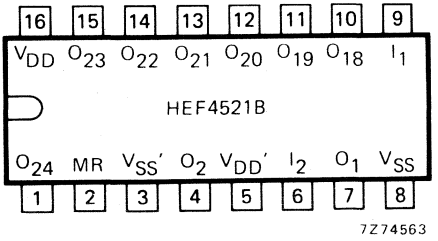


Waveforms showing set-up times for CP_0 to $\overline{CP}_1$ and $\overline{CP}_1$ to CP_0. Set-up times are shown as positive values but may be specified as negative values.

24-STAGE FREQUENCY DIVIDER

The HEF4521B consists of a chain of 24 toggle flip-flops with an overriding asynchronous master reset input (MR), and an input circuit that allows three modes of operation. The input I_2 will function as a crystal oscillator, in combination with I_1 as an RC oscillator, or as an input buffer for an external oscillator. Each flip-flop divides the frequency of the previous flip-flop by two, consequently the HEF4521B will count up to $2^{24} = 16\,777\,216$. The counting advances on the HIGH to LOW transition of the clock (I_2). The outputs of the last seven stages are available for additional flexibility.



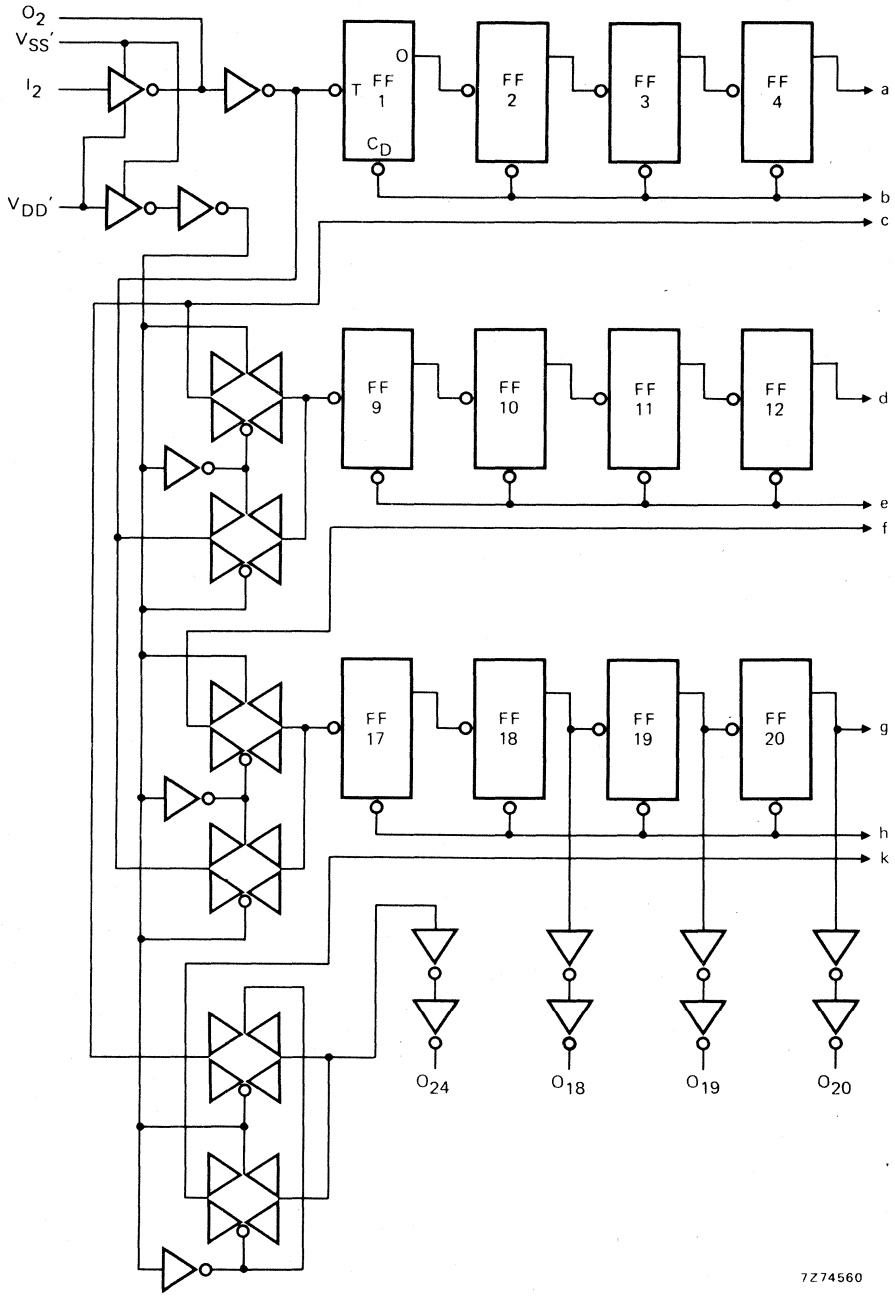


HEF4521BP : 16-lead DIL; plastic (SOT-38Z).
HEF4521BD: 16-lead DIL; ceramic (SOT-74).

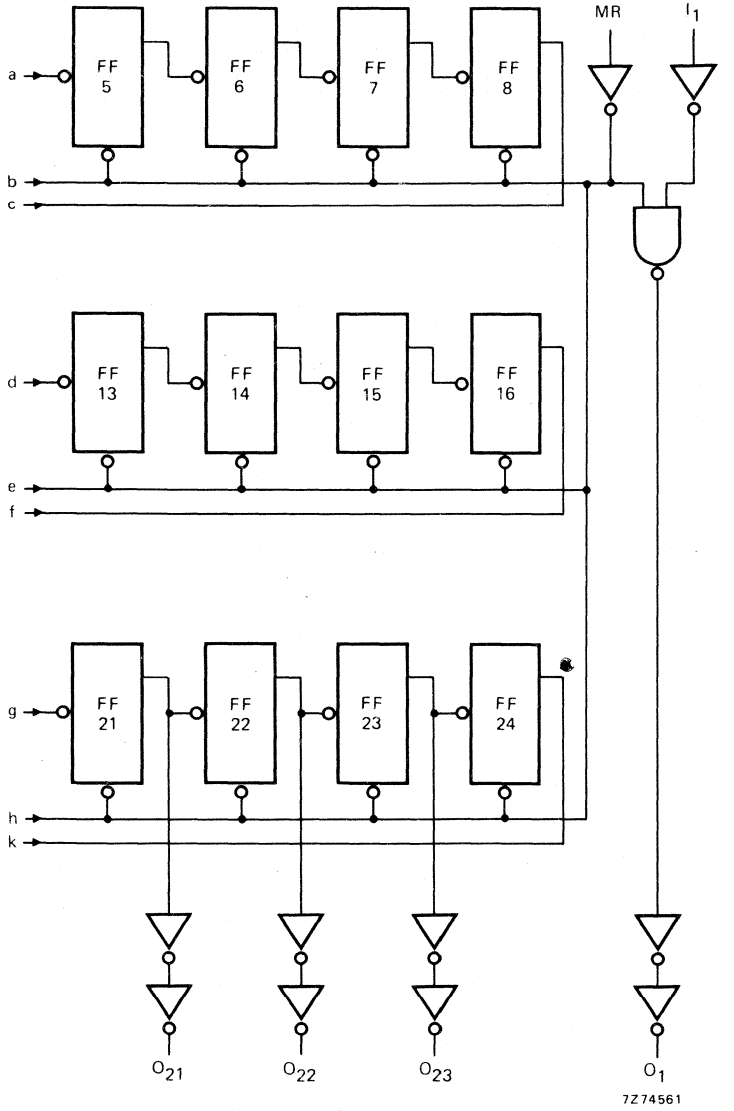
FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications


O2
VSS'
I2
VDD'
T
FF 1
O
CD
FF 2
FF 3
FF 4
a
b
c
FF 9
FF 10
FF 11
FF 12
d
e
f
FF 17
FF 18
FF 19
FF 20
g
h
k
O24
O18
O19
O20
7Z74560

DEVELOPMENT SAMPLE DATA



FUNCTIONAL TEST SEQUENCE

inputs		outputs				remarks
MR	I_2	O_2	V_{SS}'	V_{DD}'	O_{18} to O_{24}	
H	L	L	V_{DD}	V_{SS}	L	counter is in three 8-stage sections in parallel mode; counter is reset; I_2 and O_2 are interconnected
L	∫	∫	V_{DD}	V_{SS}		255 LOW to HIGH transitions are clocked into I_2, O_2 node
L	H	H	V_{DD}	V_{SS}	H	the 255th LOW to HIGH transition
L	L	L	V_{DD}	V_{SS}	H	
L	L	L	V_{SS}	V_{SS}	H	
L	H	L	V_{SS}	V_{DD}	H	counter converted back to 24-stage in series mode
L	H		V_{SS}	V_{DD}	H	O_2 converts back to an output
L	L		V_{SS}	V_{DD}	L	counter ripples from an all HIGH state to an all LOW state

A test function has been included for the reduction of the test time required to exercise all 24 counter stages. This test function divides the counter into three 8-stage sections by connecting V_{SS}' to V_{DD} and V_{DD}' to V_{SS}. Via I_2 (connected to O_2) 255 counts are loaded into each of the 8-stage sections in parallel. All flip-flops are now at a HIGH state. The counter is now returned to the normal 24-stage in series configuration by connecting V_{SS}' to V_{SS} and V_{DD}' to V_{DD}. One more pulse is entered into input I_2, which will cause the counter to ripple from an all HIGH state to an all LOW state.

COUNT CAPACITY

output	count capacity
O_{18}	$2^{18} = 262\,144$
O_{19}	$2^{19} = 524\,288$
O_{20}	$2^{20} = 1\,048\,576$
O_{21}	$2^{21} = 2\,097\,152$
O_{22}	$2^{22} = 4\,194\,304$
O_{23}	$2^{23} = 8\,388\,608$
O_{24}	$2^{24} = 16\,777\,216$

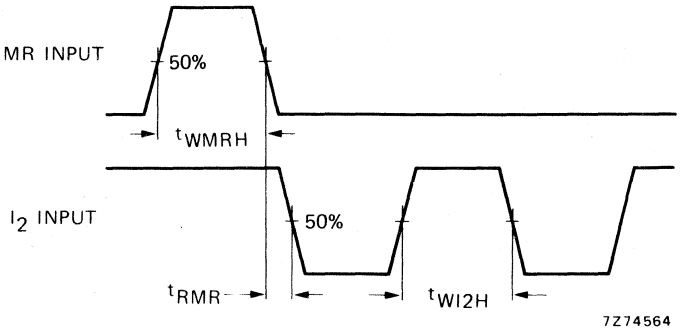
DEVELOPMENT SAMPLE DATA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Propagation delays						
$I_2 \rightarrow O_{18}$	5			1100	ns	
HIGH to LOW	10	t_{PHL}		400	ns	
	15			275	ns	
	5			1100	ns	
LOW to HIGH	10	t_{PLH}		400	ns	
	15			275	ns	
$I_1 \rightarrow O_1$	5			80	ns	
HIGH to LOW	10	t_{PHL}		35	ns	
	15			25	ns	
	5			80	ns	
LOW to HIGH	10	t_{PLH}		35	ns	
	15			25	ns	
$MR \rightarrow O_n$	5			180	ns	
HIGH to LOW	10	t_{PHL}		90	ns	
	15			70	ns	
Minimum I_2 pulse	5			25	ns	
width; HIGH	10	t_{WI2H}		15	ns	
	15			10	ns	
Minimum MR	5			65	ns	
pulse width; HIGH	10	t_{WMRH}		50	ns	
	15			45	ns	see also waveforms on page 6
Recovery time	5			60	ns	
for MR	10	t_{RMR}		35	ns	
	15			25	ns	
Maximum clock	5			10	MHz	
pulse frequency	10	f_{max}		25	MHz	
	15			35	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



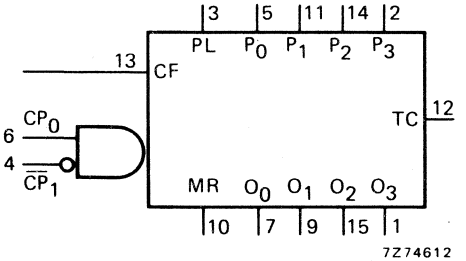
Waveforms showing minimum pulse widths for MR and I_2, recovery time for MR.

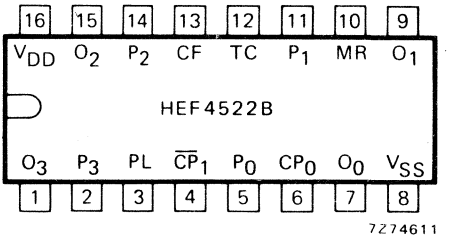
PROGRAMMABLE 4-BIT BCD DOWN COUNTER

The HEF4522B is a synchronous programmable 4-bit BCD down counter with an active HIGH and an active LOW clock input (CP_0, $\overline{CP}_1$), an asynchronous parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a decoded TC output for divide-by-n applications. In single stage applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and $\overline{CP}_1$ are LOW, the counter advances on a LOW to HIGH transition of CP_0. When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP}_1$. TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3$ = LOW) and CF is HIGH. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of other input conditions.





HEF4522BP : 16-lead DIL; plastic (SOT-38Z).
HEF4522BD: 16-lead DIL; ceramic (SOT-74).

PINNING

PL	parallel load input
P_0 to P_3	parallel inputs
CF	cascade feedback input
CP_0	clock input (LOW to HIGH, edge triggered)
$\overline{CP}_1$	clock input (HIGH to LOW, edge triggered)
MR	asynchronous master reset input
TC	terminal count output
O_0 to O_3	buffered parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

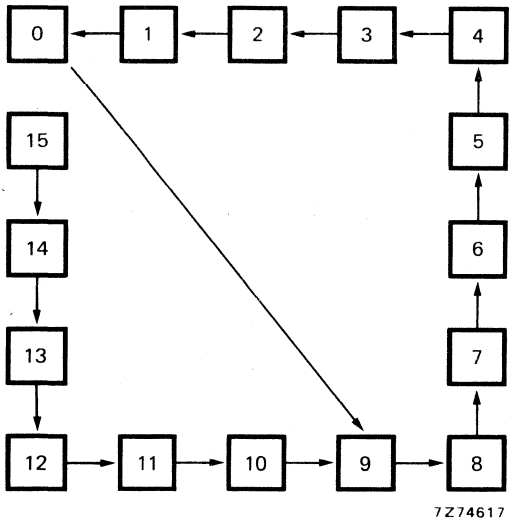
see Family Specifications

MODE SELECTION TABLE

MR	PL	CP_0	$\overline{CP}_1$	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	∫	H	no change
L	L	L	⌞	no change
L	L	⌞	X	no change
L	L	X	∫	no change
L	L	∫	L	counter advances
L	L	H	⌞	counter advances

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⌞ = negative-going transition

STATE DIAGRAM

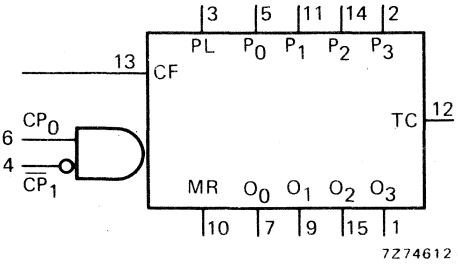


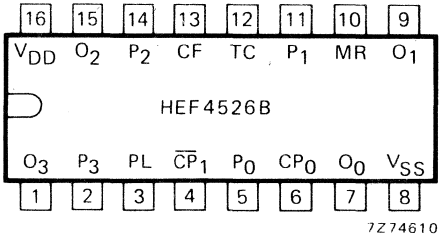
PROGRAMMABLE 4-BIT BINARY DOWN COUNTER

The HEF4526B is a synchronous programmable 4-bit binary down counter with an active HIGH and an active LOW clock input (CP_0, $\overline{CP}_1$), an **asynchronous** parallel load input (PL), four parallel inputs (P_0 to P_3), a cascade feedback input (CF), four buffered parallel outputs (O_0 to O_3), a terminal count output (TC) and an overriding asynchronous master reset input (MR).

This device is a programmable, cascadable down counter with a **decoded** TC output for divide-by-n applications. In single **stage** applications the TC output is connected to PL. CF allows cascade divide-by-n operation with no additional gates required.

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions except MR, which must be LOW. When PL and $\overline{CP}_1$ are LOW, the counter advances on a LOW to HIGH transition of CP_0. When PL is LOW and CP_0 is HIGH, the counter advances on a HIGH to LOW transition of $\overline{CP}_1$. TC is HIGH when the counter is in the zero state ($O_0 = O_1 = O_2 = O_3$ = LOW) and CF is HIGH. A HIGH on MR resets the counter (O_0 to O_3 = LOW) independent of other input conditions.





HEF4526BP: 16-lead DIL; plastic (SOT-38Z).
HEF4526BD: 16-lead DIL; ceramic (SOT-74).

PINNING

PL	parallel load input
P_0 to P_3	parallel inputs
CF	cascade feedback input
CP_0	clock input (LOW to HIGH, edge triggered)
$\overline{CP}_1$	clock input (HIGH to LOW, edge triggered)
MR	asynchronous master reset input
TC	terminal count output
O_0 to O_3	buffered parallel outputs

FAMILY DATA

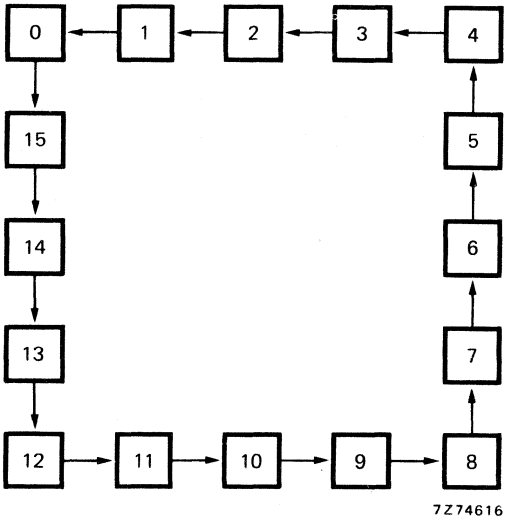
I_{DD} LIMITS category MSI } see Family Specifications

MODE SELECTION TABLE

MR	PL	CP_0	$\overline{CP}_1$	mode
H	X	X	X	reset (asynchronous)
L	H	X	X	preset (asynchronous)
L	L	∫	H	no change
L	L	L	\	no change
L	L	\	X	no change
L	L	X	∫	no change
L	L	∫	L	counter advances
L	L	H	\	counter advances

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
\ = negative-going transition

STATE DIAGRAM

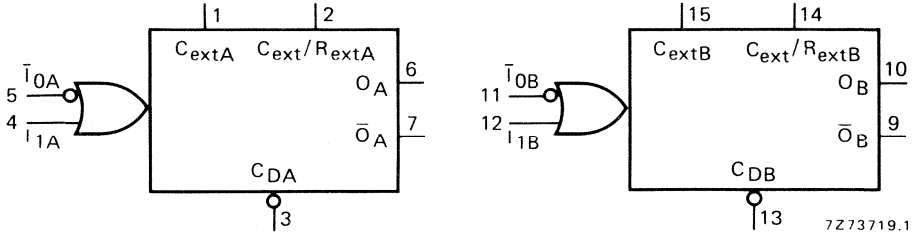


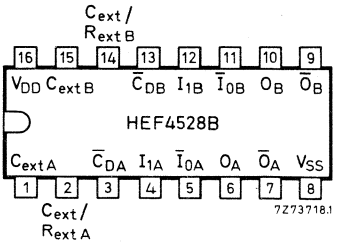
DUAL MONOSTABLE MULTIVIBRATOR

The HEF4528B is a dual retriggerable-resettable monostable multivibrator. Each multivibrator has an active LOW input ($\overline{I}_0$), and active HIGH input (I_1), an active LOW clear direct input ($\overline{C}_D$), an output (O) and its complement ($\overline{O}$), and two pins for connecting the external timing components (C_{ext}, C_{ext}/R_{ext}).

An external timing capacitor (C_t) must be connected between C_{ext} and C_{ext}/R_{ext} and an external resistor (R_t) must be connected between C_{ext}/R_{ext} and V_{DD}. The duration of the output pulse is determined by the external timing components C_t and R_t.

A HIGH to LOW transition on $\overline{I}_0$ when I_1 is LOW or a LOW to HIGH transition on I_1 when $\overline{I}_0$ is HIGH produces a positive pulse (LOW-HIGH-LOW) on O and a negative pulse (HIGH-LOW-HIGH) on $\overline{O}$ if the $\overline{C}_D$ is HIGH. A LOW on $\overline{C}_D$ forces O LOW, $\overline{O}$ HIGH and inhibits any further pulses until $\overline{C}_D$ is HIGH.





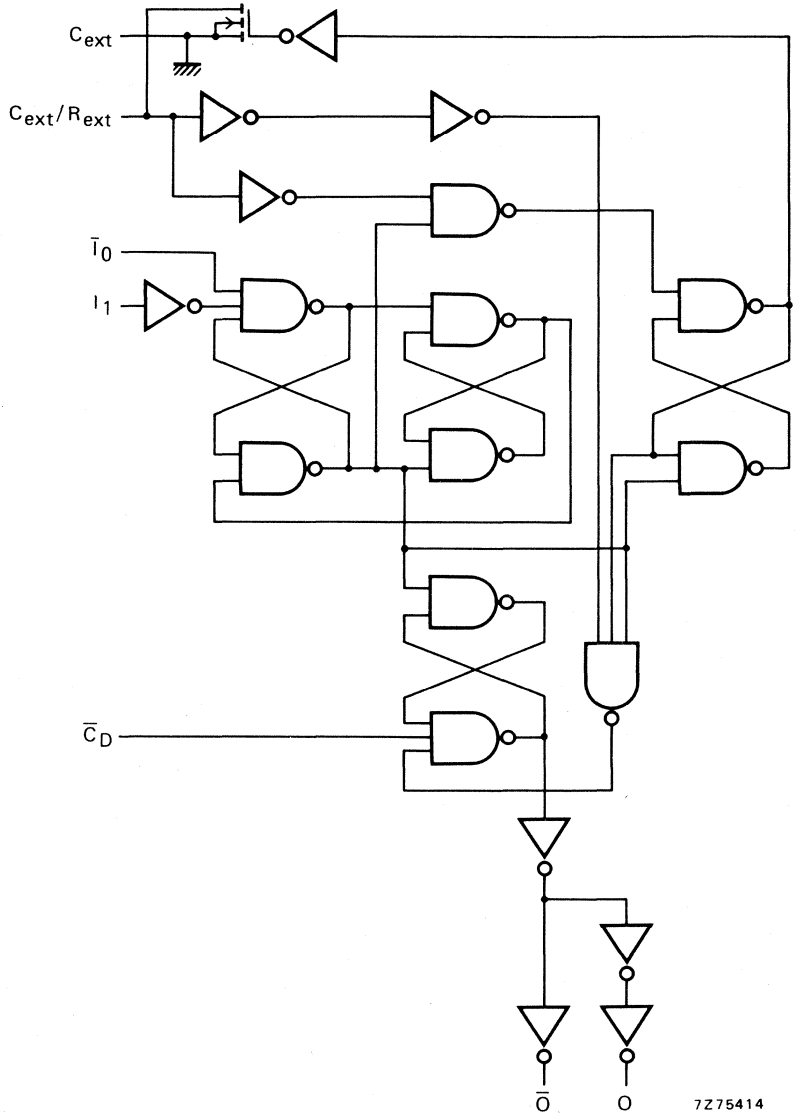
HEF4528BP : 16-lead DIL; plastic (SOT-38Z).
HEF4528BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM (one monostable multivibrator)



PINNING

$\overline{I}_{0A}$, $\overline{I}_{0B}$	input (HIGH to LOW triggered)
I_{1A}, I_{1B}	input (LOW to HIGH triggered)
$\overline{C}_{DA}$, $\overline{C}_{DB}$	clear direct input (active LOW)
O_A, O_B	output
$\overline{O}_A$, $\overline{O}_B$	complementary output (active LOW)
$C_{ext\,A}$, $C_{ext\,B}$	external capacitor connections
$C_{ext}/R_{ext\,A}$, $C_{ext}/R_{ext\,B}$	external capacitor/resistor connections

FUNCTION TABLE

inputs			outputs	
I_0	I_1	$\overline{C}_D$	O	$\overline{O}$
↘	L	H	⎍	⎎
H	↗	H	⎍	⎎
X	X	L	L	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition
⎍⎎ = positive or negative output pulse; width is determined by C_t and R_t

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{I}_0$, I_1 → $\overline{O}$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{I}_0$, I_1 → O	5			155	305	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{C}_D$ → O	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{C}_D$ → $\overline{O}$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Recovery time for $\overline{C}_D$	5	t_{RCD}	0	−75		ns	
	10		0	−30		ns	
	15		0	−25		ns	
Minimum $\overline{I}_0$ pulse width; LOW	5	t_{WI0L}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum I_1 pulse width; HIGH	5	t_{WI1H}	50	25		ns	
	10		30	15		ns	
	15		20	10		ns	
Minimum $\overline{C}_D$ pulse width; LOW	5	t_{WCDL}	60	30		ns	
	10		35	15		ns	
	15		25	10		ns	
Set-up time $\overline{C}_D \longrightarrow \overline{I}_0$ or I_1	5	t_{su}	0	−105		ns	to avoid change in output
	10		0	−40		ns	
	15		0	−25		ns	
Output O pulse width; HIGH	5	t_{WOH}	−	235		ns	note 1
	10		−	155		ns	
	15		−	140		ns	
Output O pulse width; HIGH	5	t_{WOH}	−	5,45		μs	note 2
	10		−	4,95		μs	
	15		−	4,85		μs	
Change in output O pulse width over temperature	5	Δt_{WO}	−	±3		%	note 3
	10		−	±2		%	
	15		−	±2		%	
Change in output O pulse width over V_{DD}	5	Δt_{WO}	−	±2		%	V_{DD} ± 5%
	10		−	±1		%	
	15		−	±1		%	
External timing resistor	5	R_t	5	−	2000	kΩ	
	10		5	−	2000	kΩ	
	15		5	−	2000	kΩ	
External timing capacitor	5	C_t	no limits				
	10		no limits				
	15		no limits				

For notes see page 5.

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns; R_t = 5 kΩ; C_t = 15 pF

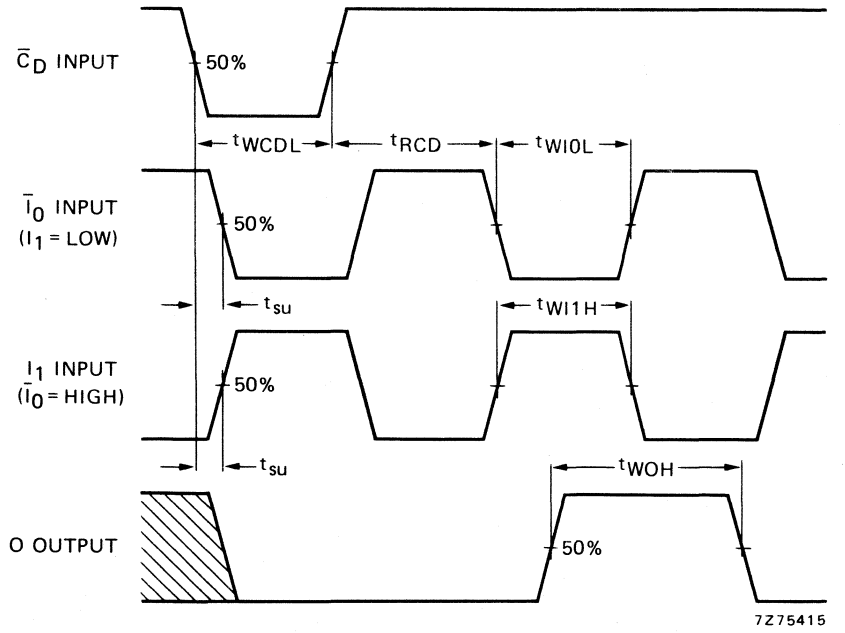
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$20\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$59\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

Notes from page 4

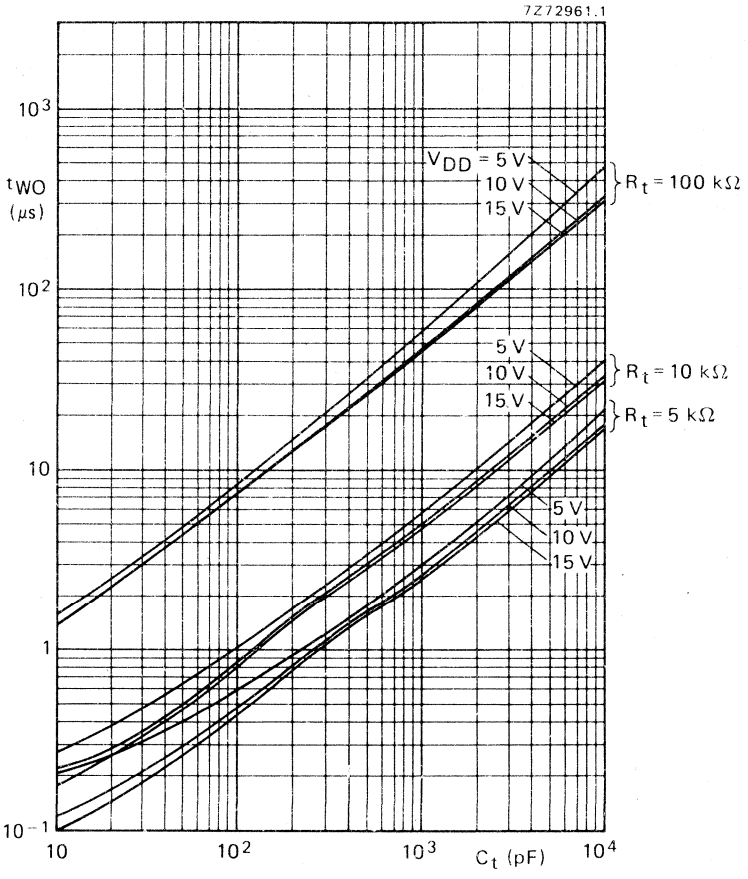
1. R_t = 5 kΩ; C_t = 15 pF; for other R_t, C_t combinations and $C_t < 0{,}01$ μF see graph on page 6.
2. R_t = 10 kΩ; C_t = 1000 pF; for other R_t, C_t combinations and $C_t > 0{,}01$ μF use formula $t_{WO} = K.R_t.C_t$.

   where: t_{WO} = output pulse width (s)
   R_t = external timing resistor (Ω)
   C_t = external timing capacitor (F)

   K = 0,42 for V_{DD} = 5 V
   K = 0,32 for V_{DD} = 10 V
   K = 0,30 for V_{DD} = 15 V
3. T_{amb} = −40 to +85 °C; Δt_{WO} is referenced to t_{WO} at T_{amb} = 25 °C.



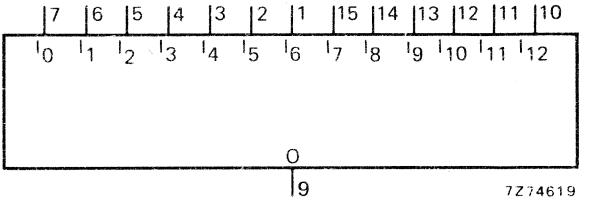
Waveforms showing minimum $\overline{I}_0$, I_1 and O pulse widths, set-up and recovery times. Set-up and recovery times are shown as positive values but may be specified as negative values.

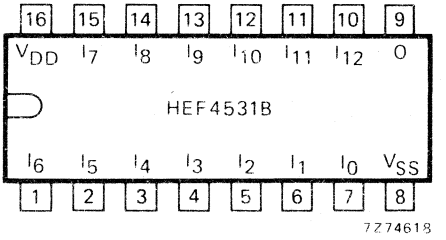


Output pulse width (t_{WO}) as a function of external timing capacitor (C_t).

13-INPUT PARITY CHECKER/GENERATOR

The HEF4531B is a parity checker/generator with 13 parity inputs (I_0 to I_{12}) and a parity output (O). When the number of parity inputs that are HIGH is even, the output is LOW. When the number of parity inputs that are HIGH is odd, the output is HIGH. For words of 12 bits or less, the output can be used to generate either odd or even parity by appropriate termination of the unused parity input(s). For words of 14 or more bits, the devices can be cascaded by connecting the output of one device to any parity input of another device. When cascading devices, it is recommended that the output of one device be connected to the I_{12} input of the other device since there is less delay to the output from the I_{12} input than from any other input (I_0 to I_{11}).



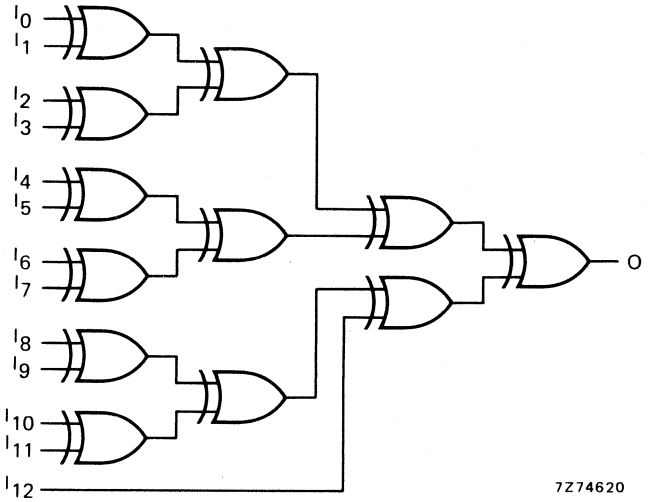


HEF4531BP : 16-lead DIL; plastic (SOT-38Z).
HEF4531BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

inputs													output
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	I_{10}	I_{11}	I_{12}	O
L	L	L	L	L	L	L	L	L	L	L	L	L	L
			any odd number of inputs HIGH										H
			any even number of inputs HIGH										L
H	H	H	H	H	H	H	H	H	H	H	H	H	H

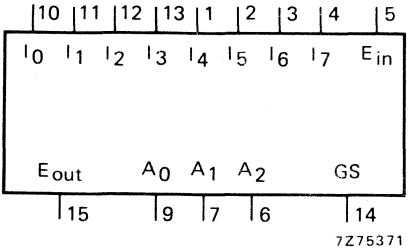
A.C. CHARACTERISTICS

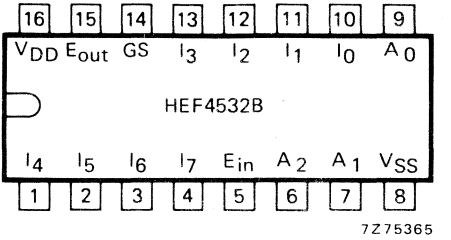
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max	
Propagation delays					
I_0 to I_{11} → O	5		195		ns
HIGH to LOW	10	t_{PHL}	80		ns
	15		55		ns
	5		195		ns
LOW to HIGH	10	t_{PLH}	80		ns
	15		55		ns
I_{12} → O	5		115		ns
HIGH to LOW	10	t_{PHL}	50		ns
	15		35		ns
	5		115		ns
LOW to HIGH	10	t_{PLH}	50		ns
	15		35		ns

8-INPUT PRIORITY ENCODER

The HEF4532B is an 8-input priority encoder with eight active HIGH priority inputs (I_0 to I_7), three active HIGH address outputs (A_0 to A_2), an active HIGH enable input (E_{in}), an active HIGH enable output (E_{out}) and an active HIGH group select output (GS).
Data is accepted on inputs I_0 to I_7. The binary code corresponding to the highest priority input (I_0 to I_7) which is HIGH, is generated on A_0 to A_2 if E_{in} is HIGH. Input I_7 is assigned the highest priority. GS is HIGH when one or more priority inputs and E_{in} are HIGH. E_{out} is HIGH when I_0 to I_7 are LOW and E_{in} is HIGH. E_{in}, when LOW, forces all output (A_0 to A_2, GS, E_{out}) LOW.





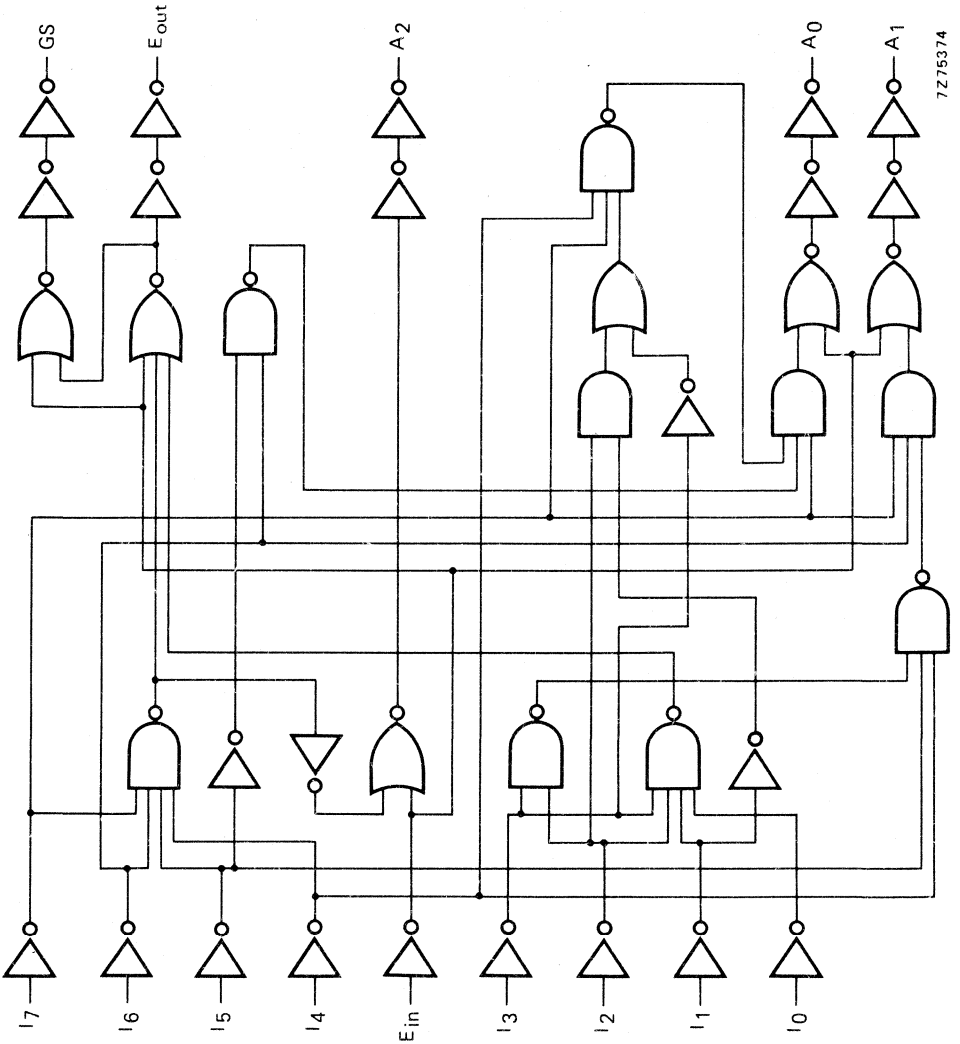
HEF4532BP: 16-lead DIL; plastic (SOT-38Z).
HEF4532BD: 16-lead DIL; ceramic (SOT-74).

PINNING

I_0 to I_7	priority inputs
E_{in}	enable input
E_{out}	enable output
GS	group select output
A_0 to A_2	address outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications



LOGIC DIAGRAM

TRUTH TABLE

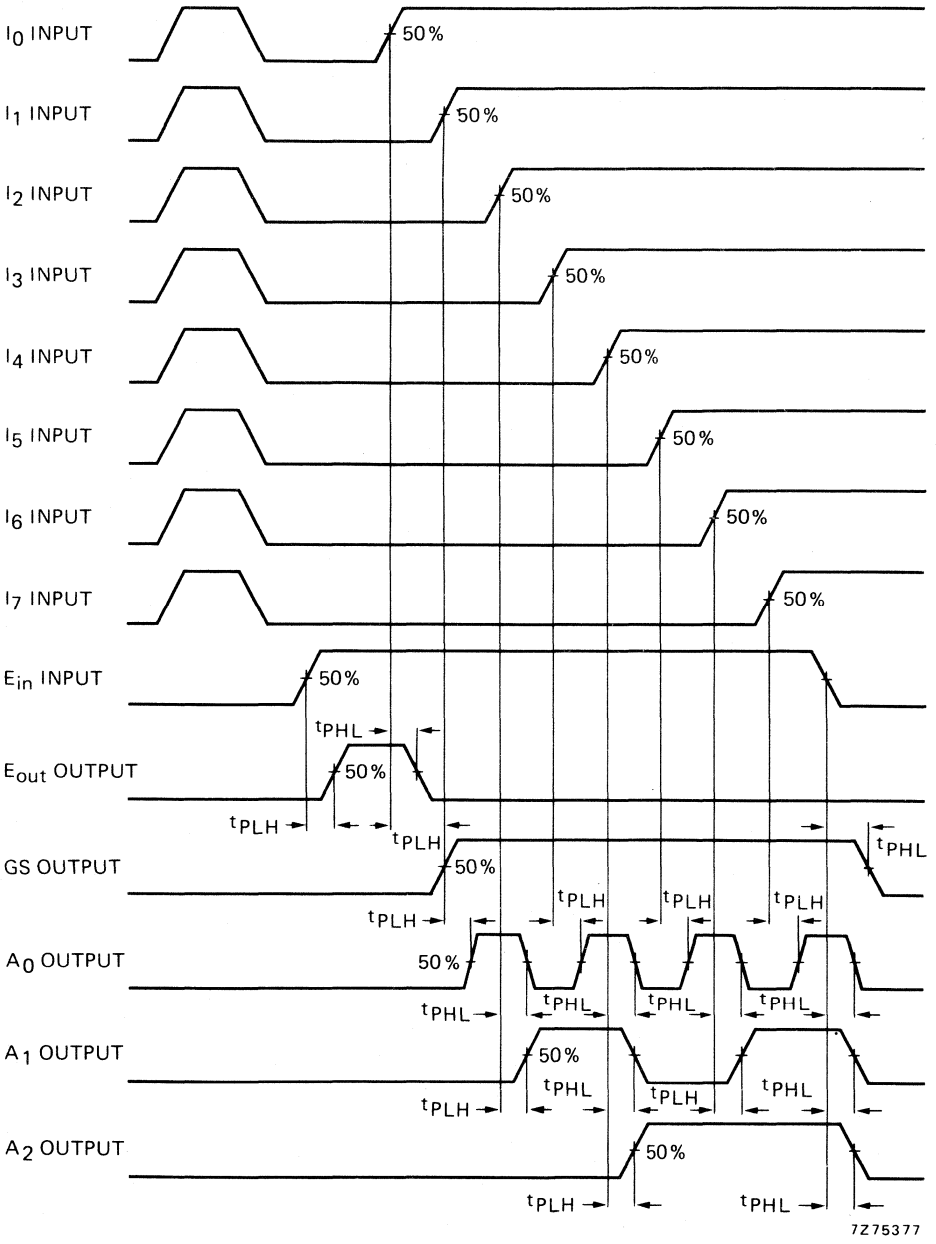
inputs									outputs				
E_{in}	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	GS	A_2	A_1	A_0	E_{out}
L	X	X	X	X	X	X	X	X	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	L	L	H
H	H	X	X	X	X	X	X	X	H	H	H	H	L
H	L	H	X	X	X	X	X	X	H	H	H	L	L
H	L	L	H	X	X	X	X	X	H	H	L	H	L
H	L	L	L	H	X	X	X	X	H	H	L	L	L
H	L	L	L	L	H	X	X	X	H	L	H	H	L
H	L	L	L	L	L	H	X	X	H	L	H	L	L
H	L	L	L	L	L	L	H	X	H	L	L	H	L
H	L	L	L	L	L	L	L	H	H	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Propagation delays						
E_{in} → E_{out}	5			85		ns
HIGH to LOW	10	t_{PHL}		45		ns
	15			35		ns
	5			85		ns
LOW to HIGH	10	t_{PLH}		45		ns
	15			35		ns
E_{in} → GS	5			65		ns
HIGH to LOW	10	t_{PHL}		35		ns
	15			25		ns
	5			65		ns
LOW to HIGH	10	t_{PLH}		35		ns
	15			25		ns
E_{in} → A_n	5			135		ns
HIGH to LOW	10	t_{PHL}		70		ns
	15			45		ns
	5			135		ns
LOW to HIGH	10	t_{PLH}		70		ns
	15			45		ns
I_n → A_n	5			135		ns
HIGH to LOW	10	t_{PHL}		70		ns
	15			50		ns
	5			135		ns
LOW to HIGH	10	t_{PLH}		70		ns
	15			50		ns
I_n → GS	5			135		ns
HIGH to LOW	10	t_{PHL}		60		ns
	15			45		ns
	5			135		ns
LOW to HIGH	10	t_{PLH}		60		ns
	15			45		ns
Transition times	5			60		ns
HIGH to LOW	10	t_{THL}		30		ns
	15			20		ns
	5			60		ns
LOW to HIGH	10	t_{TLH}		30		ns
	15			20		ns



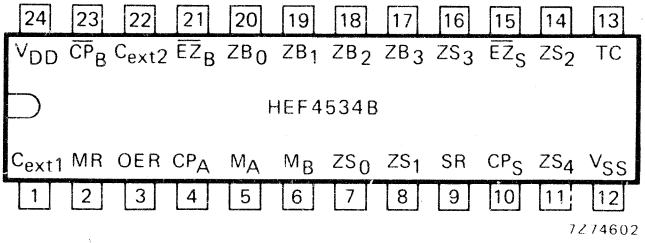
Waveforms showing propagation delays from inputs to outputs.

REAL TIME 5-DECADE COUNTER

The HEF4534B is a 5-decade ripple counter. The binary outputs of the decade counters are time-multiplexed by an internal scanner on four BCD outputs (ZB_0 to ZB_3). The selected decade is indicated by a logic HIGH on the appropriate digit select output (ZS_0: units, 1; ZS_1: tens, 10; ZS_2: hundreds, 10^2; ZS_3: thousands, 10^3; ZS_4: ten thousands, 10^4).

The binary outputs (ZB_0 to ZB_3) and the select outputs (ZS_0 to ZS_4) are 3-state controlled via enable inputs $\overline{EZ}_B$ and $\overline{EZ}_S$ respectively. Cascading may be accomplished by using the carry out (TC). The counter is triggered by a LOW to HIGH transition on the decade clock (CP_A) and is reset by a HIGH level on the master reset (MR). The scanner is triggered by a LOW to HIGH transition on the scanner clock (CP_S) and is reset (select ten thousand counter) by a HIGH level on the scanner reset (SR).

The counter can operate in four modes depending on the state of the mode inputs (M_A, M_B). The error detector will detect an error when a positive edge on CP_A is not accompanied by a negative edge on $\overline{CP}_B$ or vice versa, within time limits adjusted by external capacitors connected to C_{ext1} and C_{ext2}. Three or more detected errors result in a HIGH level on the error output (OER). The error detector is reset by a HIGH level on MR.

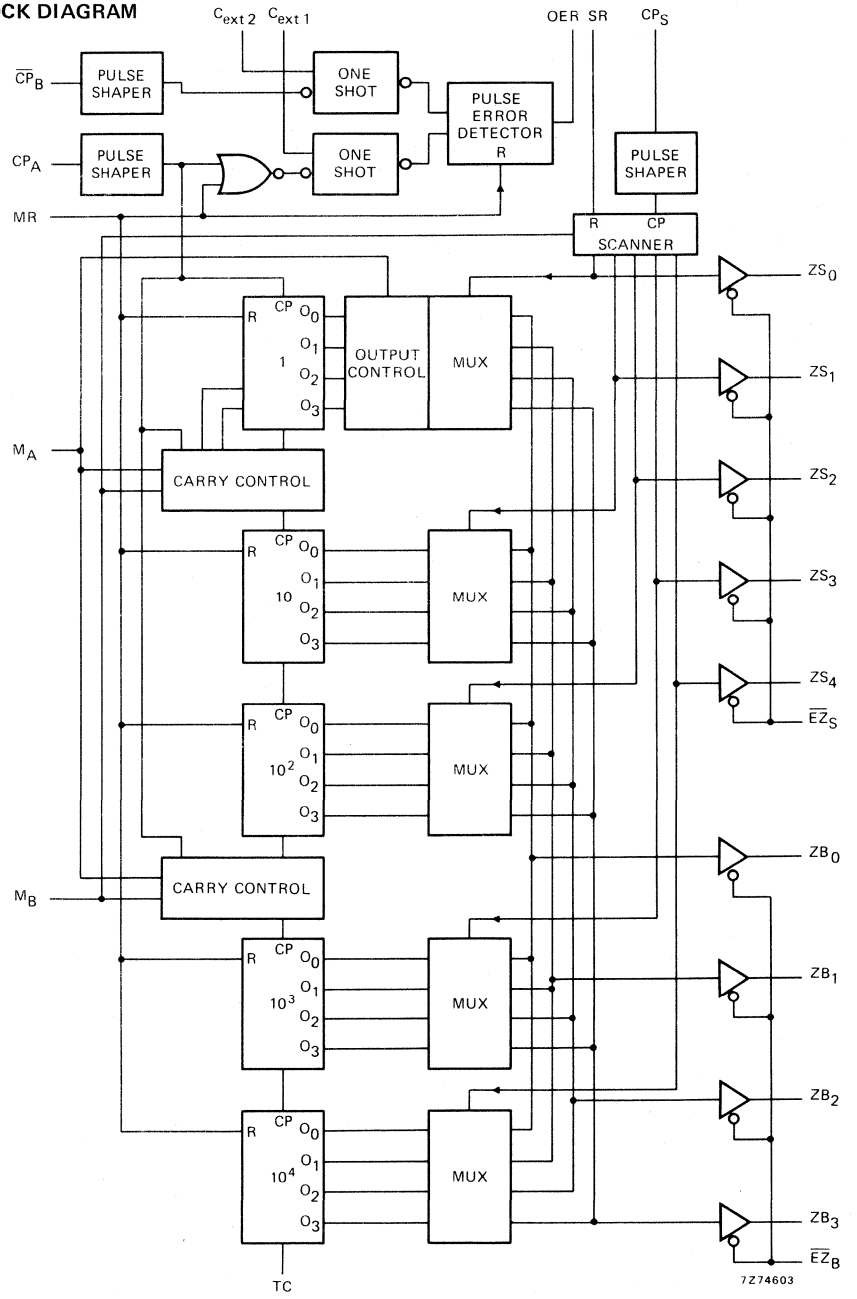


HEF4534BP: 24-lead DIL; plastic (SOT-101A).
HEF4534BD: 24-lead DIL; ceramic (SOT-94).

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 3

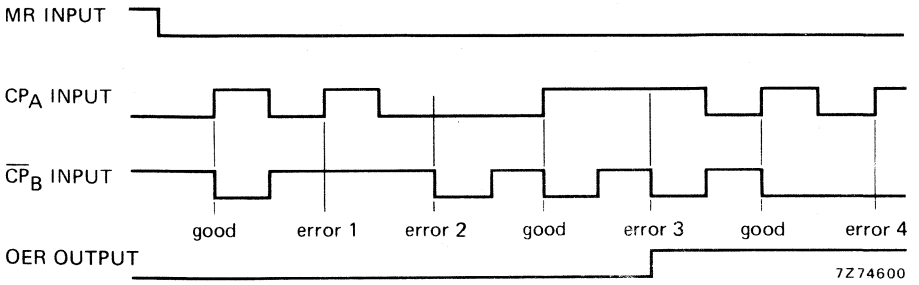
BLOCK DIAGRAM



MODE CONTROL FUNCTION TABLE

M_A	M_B	1st decade output	carry to 2nd stage	carry to 4th stage
L	L	normal count and display	at 9 to 0 transition of the 1st decade	at 9 to 0 transition of the 3rd decade
L	H	inhibited	input clock	input clock
H	H	inhibited	at 4 to 5 transition of the 1st decade	at 9 to 0 transition of the 3rd decade
H	L	displays: 3, 4, 5, 6, 7 = 5 8, 9, 0, 1, 2 = 0	at 7 to 8 transition of the 1st decade	at 9 to 0 transition of the 3rd decade

ERROR DETECTION TIMING DIAGRAM



D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 typ	−40 max	+25 min	+25 typ	+25 max	+85 min	+85 typ	+85 max	
Output current LOW at C_{ext1}, C_{ext2}	5	5	I_{OL}					0,12					mA
	10	10						0,6					mA
	15	15						1,8					mA
Quiescent device current	5		I_{DD}				50		50			375	μA
	10						100		100			750	μA
	15						200		200			1500	μA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Propagation delays						
CP_A → ZB_n	5			2000		ns
HIGH to LOW	10	t_{PHL}		750		ns
	15			600		ns
	5			2000		ns
LOW to HIGH	10	t_{PLH}		750		ns
	15			600		ns
CP_A → TC	5			1600		ns
LOW to HIGH	10	t_{PLH}		500		ns
	15			400		ns
MR → ZB_n	5			900		ns
HIGH to LOW	10	t_{PHL}		300		ns
	15			250		ns
MR → OER	5			300		ns
HIGH to LOW	10	t_{PHL}		100		ns
	15			80		ns
CP_S → ZB_n	5			900		ns
HIGH to LOW	10	t_{PHL}		300		ns
	15			250		ns
	5			900		ns
LOW to HIGH	10	t_{PLH}		300		ns
	15			250		ns
CP_S → ZS_n	5			750		ns
HIGH to LOW	10	t_{PHL}		250		ns
	15			200		ns
	5			750		ns
LOW to HIGH	10	t_{PLH}		250		ns
	15			200		ns

A.C. CHARACTERISTICS

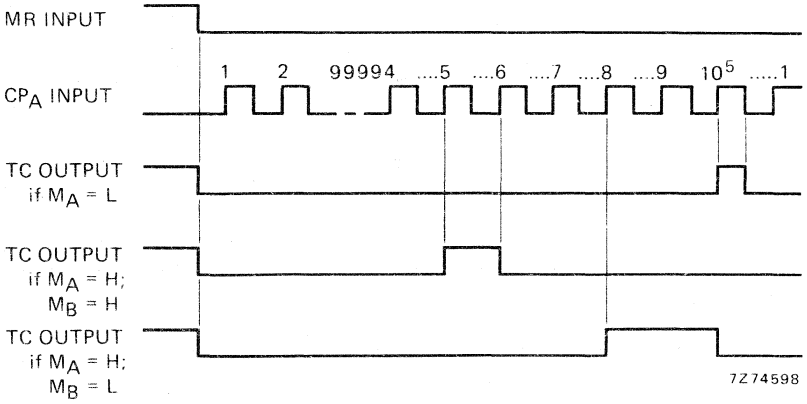
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Minimum clock pulse width; HIGH CP_A, CP_S	5	t_{WCPH}		250	ns	
	10			100	ns	
	15			80	ns	
Minimum reset pulse width; HIGH MR, SR	5	t_{WRH}		500	ns	
	10			200	ns	
	15			160	ns	
Minimum error skew time between CP_A and $\overline{CP}_B$	5	t_{SK}		2000	ns	notes 1 and 2
	10			900	ns	
	15			600	ns	
Maximum non-error skew time between CP_A and $\overline{CP}_B$	5	t_{SK}		2000	ns	notes 1 and 3
	10			900	ns	
	15			600	ns	
Maximum clock pulse frequency CP_A and CP_S	5	f_{max}		2	MHz	
	10			5	MHz	
	15			10	MHz	

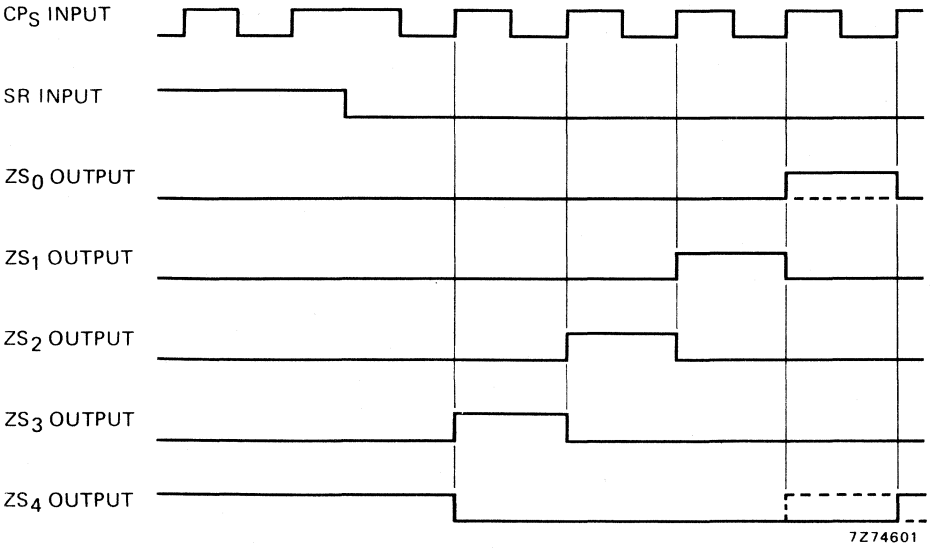
NOTES

1. The skew time is the time difference between the LOW to HIGH transition of CP_A and the HIGH to LOW transition of $\overline{CP}_B$ or vice versa. The skew time is typically proportional to the external capacitor (C_{ext}) connected between C_{ext1} and C_{ext2} and V_{SS} ($C_{ext} > 100$ pF). The skew times are specified at C_{ext} = 100 pF.
2. The error skew time results in a counted error.
3. The non-error skew time results in no error counted.

CARRY TIMING DIAGRAM

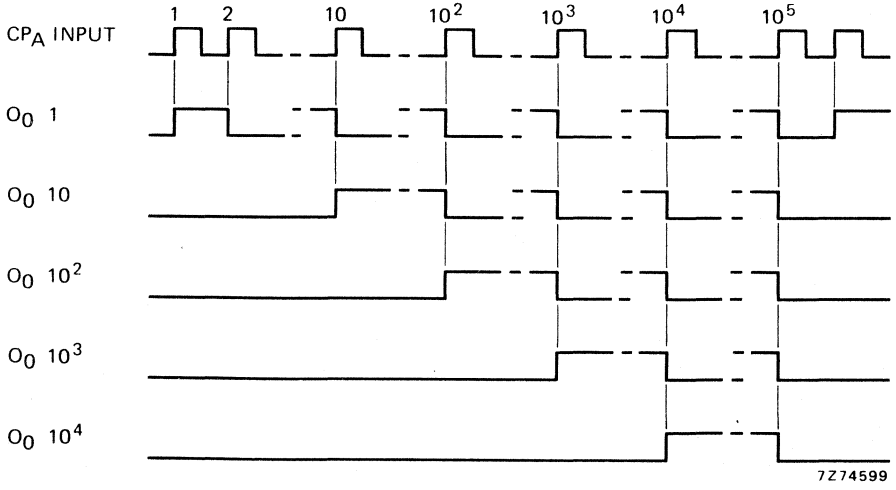


SCANNER TIMING DIAGRAM



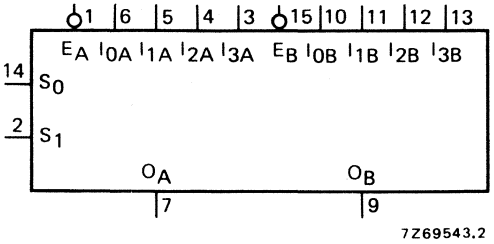
Note: If MB = H, the 1st decade is inhibited and the cycle will be shortened to four stages (see dotted lines).

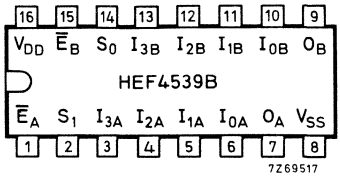
COUNTER TIMING DIAGRAM



DUAL 4-INPUT MULTIPLEXER

The HEF4539B is a dual 4-input multiplexer with common select logic. Each multiplexer has four multiplexer inputs (I_0 to I_3), an active LOW enable input ($\overline{E}$) and a multiplexer output (O). When HIGH, $\overline{E}$ forces O of the respective multiplexer LOW, independent of the select inputs (S_0 and S_1) and I_0 to I_3. When $\overline{E}$ is LOW, S_0 and S_1 determine which multiplexer input (I_0 to I_3) on each of the multiplexers is routed to the respective multiplexer output (O).





HEF4539BP: 16-lead DIL; plastic (SOT-38Z).
HEF4539BD: 16-lead DIL; ceramic (SOT-74).

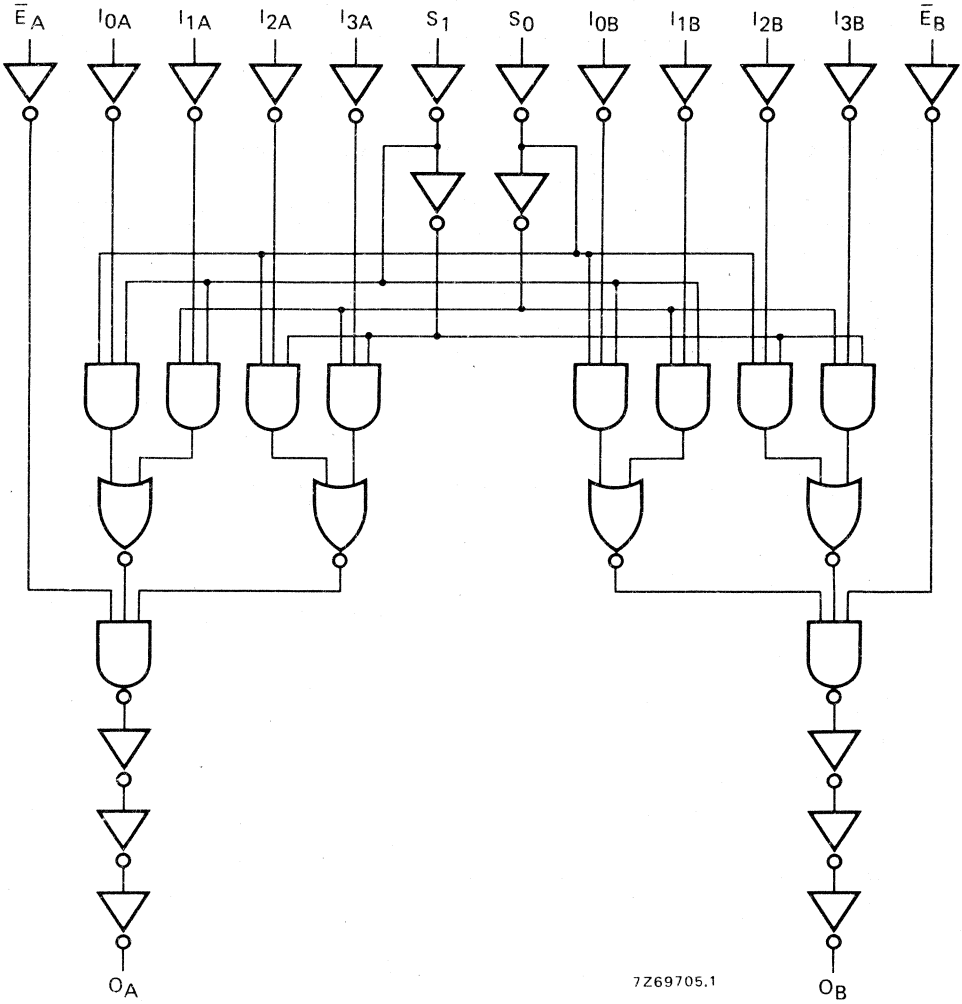
PINNING

I_{0A}, I_{1A}, I_{2A}, I_{3A}	multiplexer inputs
I_{0B}, I_{1B}, I_{2B}, I_{3B}	multiplexer inputs
S_0, S_1	select inputs
$\overline{E}_A$, $\overline{E}_B$	enable inputs (active LOW)
O_A, O_B	multiplexer outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

inputs			output
S_0	S_1	$\overline{E}_n$	O_n
X	X	H	L
L	L	L	I_0
H	L	L	I_1
L	H	L	I_2
H	H	L	I_3

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

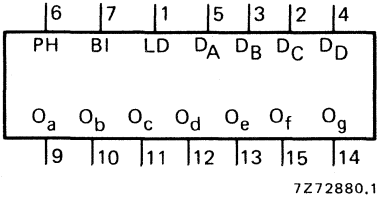
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$I_n \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
$S_n \rightarrow O_n$	5			165	330	ns	138 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		65	125	ns	54 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			155	310	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2900 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	8100 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

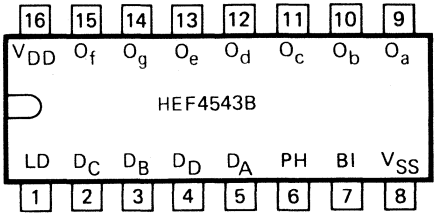
BCD TO 7-SEGMENT LATCH/DECODER/DRIVER

The HEF4543B is a BCD to 7-segment latch/decoder/driver for liquid crystal and LED displays. The circuit provides the function of a 4-bit storage latch and an 8-4-2-1 BCD to 7-segment decoder/driver. It can invert the logic levels of the output combination. The phase (PH), blanking (BI) and latch disable (LD) inputs are used to reverse the function table phase, blank the display and store a BCD code, respectively.

For liquid crystal displays a square-wave is applied to PH and the electrical common back-plane of the display. The outputs of the device are directly connected to the segments of the liquid crystal.



7Z72880.1



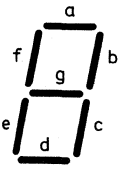
7Z72881.1

HEF4543BP: 16-lead DIL; plastic (SOT-38Z).
HEF4543BD: 16-lead DIL; ceramic (SOT-74).

PINNING

D_A to D_D	address (data) inputs
PH	phase input (active HIGH)
BI	blanking input (active HIGH)
LD	latch disable input (active HIGH)
O_a to O_g	segment outputs

SEGMENT DESIGNATION

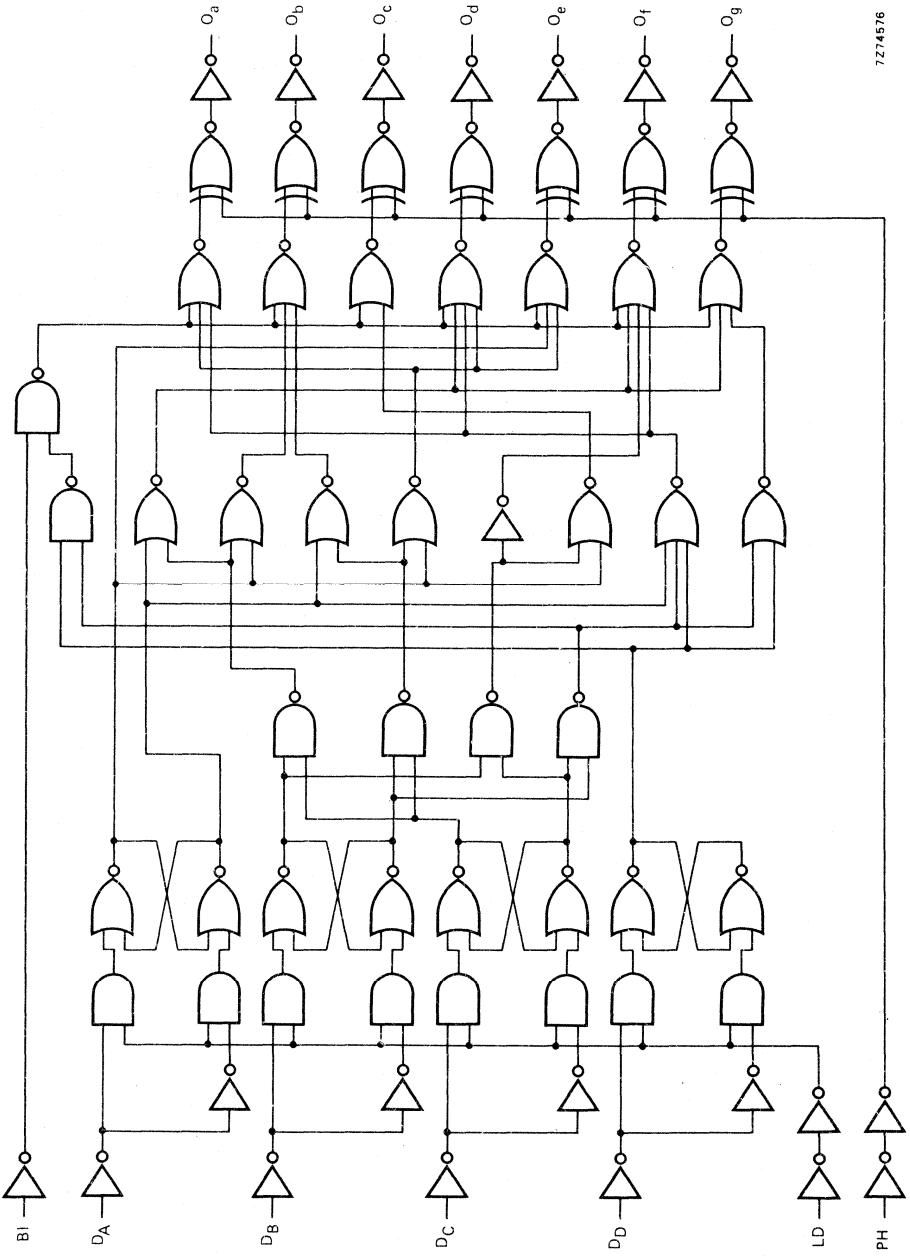


FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



FUNCTION TABLE

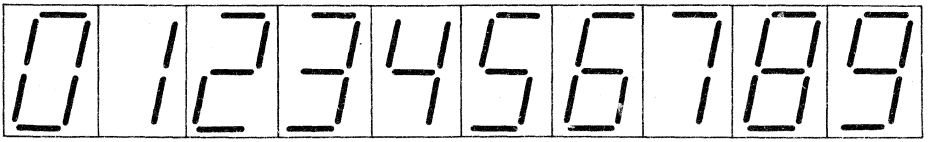
inputs							outputs							
LD	BI	PH *	D_D	D_C	D_B	D_A	O_a	O_b	O_c	O_d	O_e	O_f	O_g	display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	blank
L	L	L	X	X	X	X				* *				* *
as above		H	as above				inverse of above							as above

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

* For liquid crystal displays, apply a square-wave to PH.
For common cathode LED displays, select PH = LOW.
For common anode LED displays, select PH = HIGH.

** Depends upon the BCD-code previously applied when LD = HIGH.

DISPLAY



7Z72882

A.C. CHARACTERISTICS

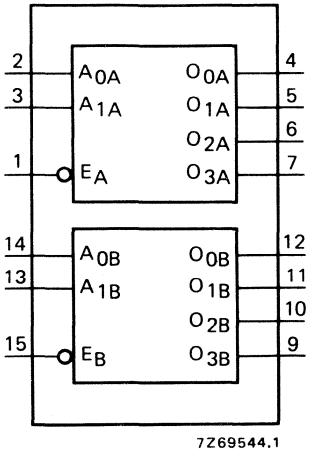
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$D_n \rightarrow O_n$	5			185	370	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	95	ns	42 ns + (0,16 ns/pF) C_L
	5			155	305	ns	128 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
$LD \rightarrow O_n$	5			205	405	ns	178 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	155	ns	64 ns + (0,23 ns/pF) C_L
	15			50	105	ns	42 ns + (0,16 ns/pF) C_L
	5			150	300	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	125	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$BI \rightarrow O_n$	5			135	265	ns	108 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			100	200	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Minimum LD	5		50	25		ns	
pulse width	10	t_{WLDH}	20	10		ns	
	15		16	8		ns	
Set-up time	5		45	20		ns	
$D_n \rightarrow LD$	10	t_{su}	15	10		ns	
	15		10	5		ns	
Hold time	5		10	−15		ns	
$D_n \rightarrow LD$	10	t_{hold}	0	−10		ns	
	15		0	−5		ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	10 900 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	40 600 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4555B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active HIGH (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 LOW. When used as a demultiplexer, the appropriate output is selected by the data on A_0 and A_1. All unselected outputs are LOW.



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7Z69518

HEF4555BP: 16-lead DIL; plastic (SOT-38Z).
HEF4555BD: 16-lead DIL; ceramic (SOT-74).

PINNING

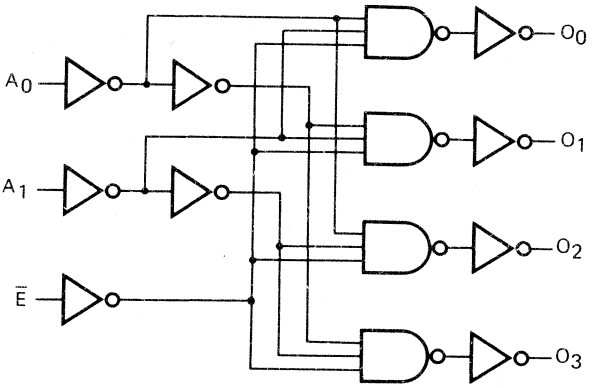
$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
O_0 to O_3	outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

inputs			outputs			
$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H
H	X	X	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

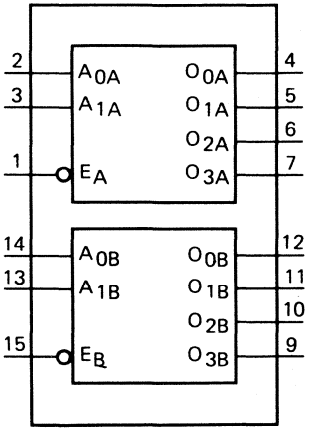
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$A_n \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			150	295	ns	123 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	75	ns	32 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	4500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	18 800 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	45 700 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

DUAL 1-OF-4 DECODER/DEMULTIPLEXER

The HEF4556B is a dual 1-of-4 decoder/demultiplexer. Each has two address inputs (A_0 and A_1), an active LOW enable input ($\overline{E}$) and four mutually exclusive outputs which are active LOW (O_0 to O_3). When used as a decoder, $\overline{E}$ when HIGH, forces O_0 to O_3 HIGH. When used as a demultiplexer, the appropriate output is selected by the data on A_0 and A_1. All unselected outputs are HIGH.



HEF4556BP: 16-lead DIL; plastic (SOT-38Z).
HEF4556BD: 16-lead DIL; ceramic (SOT-74).

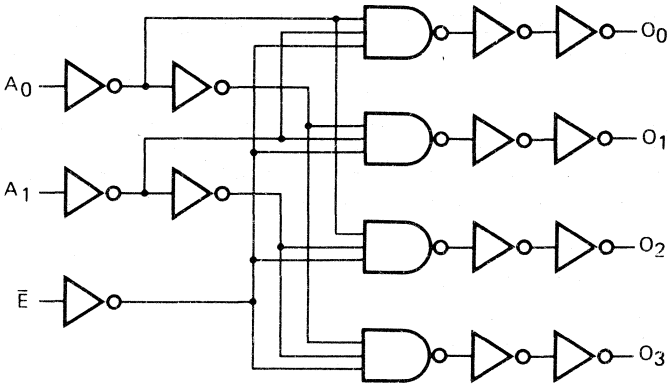
PINNING

$\overline{E}$	enable inputs (active LOW)
A_0 and A_1	address inputs
O_0 to O_3	outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

inputs			outputs			
$\bar{E}$	A_0	A_1	O_0	O_1	O_2	O_3
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L
H	X	X	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

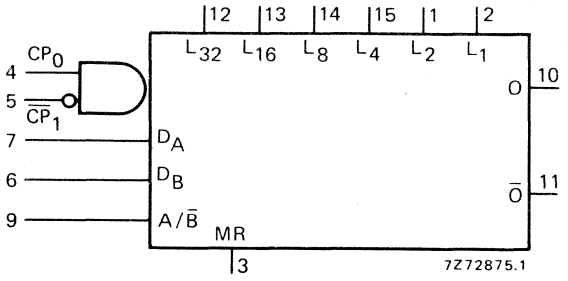
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

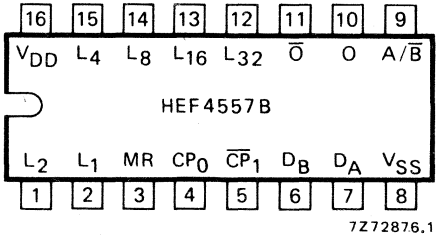
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$A_n \rightarrow O_n$	5			130	255	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$\overline{E}_n \rightarrow O_n$	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			105	205	ns	78 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$4400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$18\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$43\,300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

1-to-64 BIT VARIABLE LENGTH SHIFT REGISTER

The HEF4557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled length control inputs (L_1, L_2, L_4, L_8, L_{16} and L_{32}) plus one. Serial data may be selected from the D_A or D_B data inputs with the $A/\overline{B}$ select input. This feature is useful for recirculation purposes. Information on D_A or D_B is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP_0 while $\overline{CP}_1$ is LOW or on the HIGH to LOW transition of $\overline{CP}_1$ while CP_0 is HIGH. When HIGH master reset (MR) resets the whole register asynchronously (O = LOW; $\overline{O}$ = HIGH) and independent of the other inputs.





PINNING

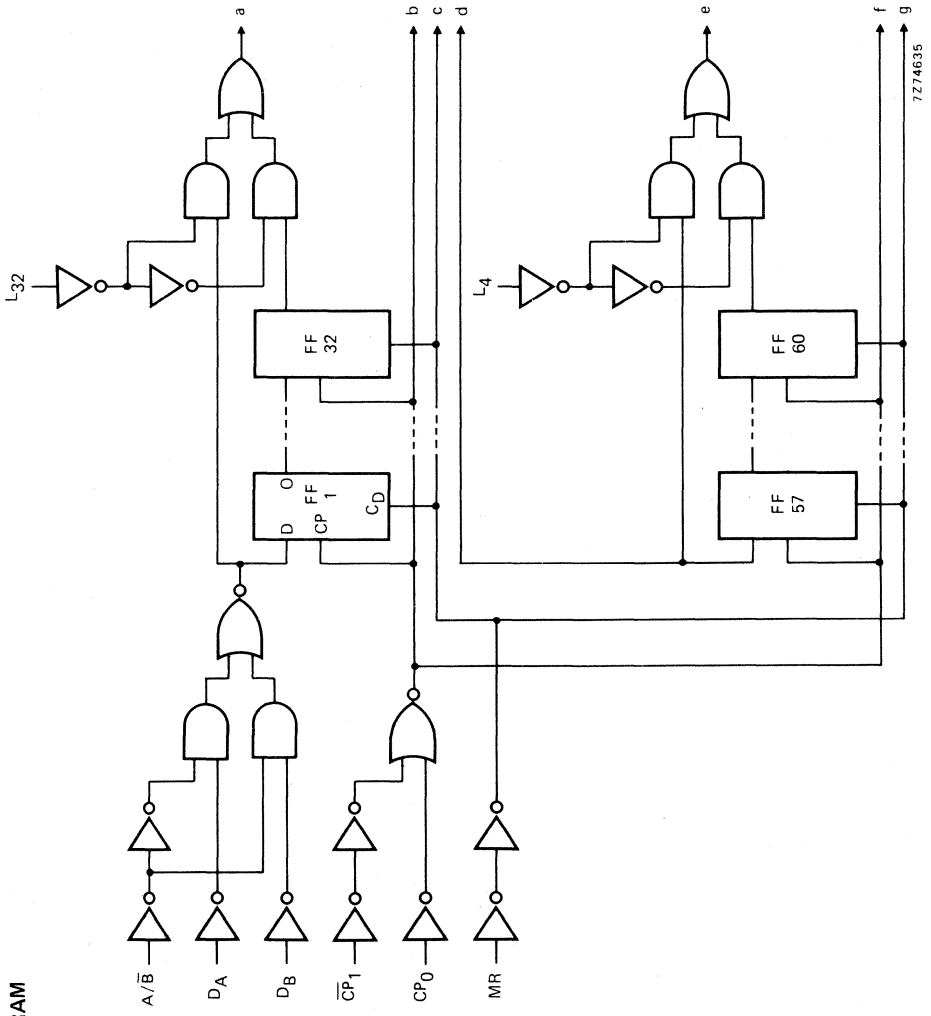
D_A, D_B	data inputs
$A/\overline{B}$	select data input
CP_0	clock input
$\overline{CP}_1$	clock enable input
MR	asynchronous master reset
L_1 to L_{32}	bit-length control inputs
O, $\overline{O}$	buffered outputs

HEF4557BP : 16-lead DIL; plastic (SOT-38Z).
HEF4557BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 4

LOGIC DIAGRAM



DEVELOPMENT SAMPLE DATA

LOGIC DIAGRAM (continued)

FUNCTION TABLE

inputs						output
MR	$A/\overline{B}$	D_A	D_B	CP_0	$\overline{CP}_1$	O *
L	L	D_1	D_2	∫	L	D_2
L	H	D_1	D_2	∫	L	D_1
L	L	D_1	D_2	H	⟍	D_2
L	H	D_1	D_2	H	⟍	D_1
H	X	X	X	X	X	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition
⟍ = negative-going transition
D_n = either HIGH or LOW

* The moment D_n appears at Q depends on the table below.

BIT-LENGTH SELECT FUNCTION TABLE

L_{32}	L_{16}	L_8	L_4	L_2	L_1	register length
L	L	L	L	L	L	1-bit
L	L	L	L	L	H	2-bits
L	L	L	L	H	L	3-bits
L	L	L	L	H	H	4-bits
L	L	L	H	L	L	5-bits
L	L	L	H	L	H	6-bits
L	L	L	H	H	L	7-bits
L	L	L	H	H	H	8-bits
↓	↓	↓	↓	↓	↓	↓
L	H	H	H	H	H	32-bits
H	L	L	L	L	L	33-bits
H	L	L	L	L	H	34-bits
↓	↓	↓	↓	↓	↓	↓
H	H	H	H	L	L	61-bits
H	H	H	H	L	H	62-bits
H	H	H	H	H	L	63-bits
H	H	H	H	H	H	64-bits

D.C. CHARACTERISTIC

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Quiescent device current	5	I_{DD}		50		50		375	μA
	10			100		100		750	μA
	15			200		200		1500	μA

A.C. CHARACTERISTICS

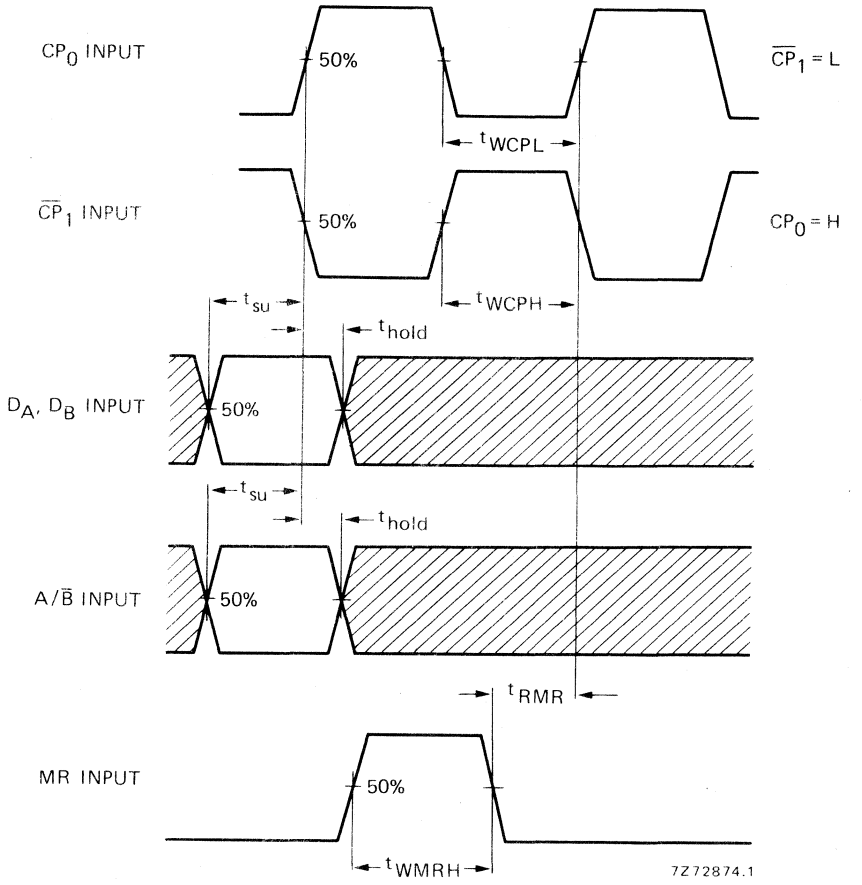
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	symbol	typ	max	typical extrapolation formula
Propagation delays					
CP_0, $\overline{CP}_1$ → O, $\overline{O}$	5		240	ns	213 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	85	ns	74 ns + (0,23 ns/pF) C_L
	15		60	ns	52 ns + (0,16 ns/pF) C_L
	5		220	ns	193 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	80	ns	69 ns + (0,23 ns/pF) C_L
	15		55	ns	47 ns + (0,16 ns/pF) C_L
MR → O, $\overline{O}$	5		170	ns	143 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	75	ns	64 ns + (0,23 ns/pF) C_L
	15		60	ns	52 ns + (0,16 ns/pF) C_L
	5		170	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	75	ns	64 ns + (0,23 ns/pF) C_L
	15		60	ns	52 ns + (0,16 ns/pF) C_L
Minimum clock pulse width;	5	t_{WCPL}	95	ns	
LOW for CP_0 or	10	or	30	ns	
HIGH for $\overline{CP}_1$	15	t_{WCPH}	20	ns	
Minimum reset	5		65	ns	
pulse width; HIGH	10	t_{WMRH}	30	ns	
	15		25	ns	
Set-up times	5		165	ns	
D_A, D_B → CP_0, $\overline{CP}_1$	10	t_{su}	60	ns	
	15		45	ns	
	5		165	ns	
A/$\overline{B}$ → CP_0, $\overline{CP}_1$	10	t_{su}	60	ns	
	15		45	ns	see also waveforms on page 6
Hold times	5		0	ns	
D_A, D_B → CP_0, $\overline{CP}_1$	10	t_{hold}	0	ns	
	15		0	ns	
	5		0	ns	
A/$\overline{B}$ → CP_0, $\overline{CP}_1$	10	t_{hold}	0	ns	
	15		0	ns	
Recovery time	5		190	ns	
for MR	10	t_{RMR}	80	ns	
	15		60	ns	
Maximum clock	5		5	MHz	
pulse frequency	10	f_{max}	14	MHz	
	15		20	MHz	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

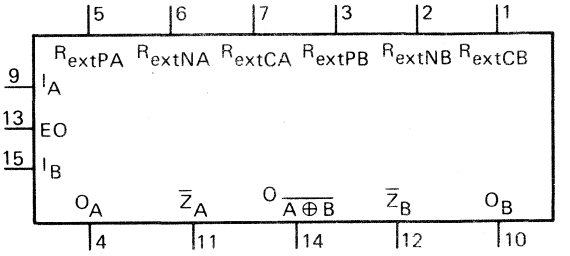
	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_oC_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$3\,000\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	10	$12\,400\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	
	15	$32\,300\ f_i + \Sigma(f_oC_L) \times V_{DD}^2$	

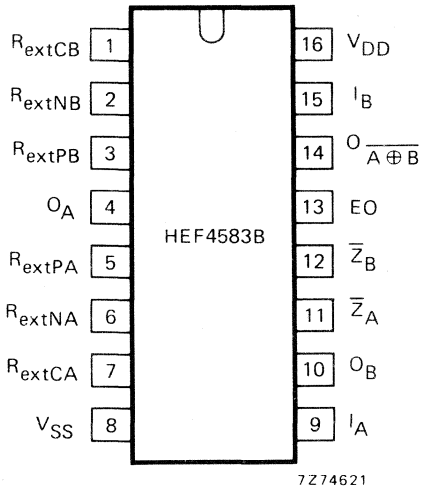


Waveforms showing recovery time for MR and minimum CP_0, $\overline{CP}_1$ and MR pulse widths, set-up and hold times for D_A, D_B and $A/\overline{B}$ to CP_0 and $\overline{CP}_1$. Set-up and hold times are shown as positive values but may be specified as negative values.

DUAL SCHMITT TRIGGER

The HEF4583B is a dual Schmitt trigger offering both positive and negative threshold voltages (V_{T+}, V_{T-}), which are programmable via $R_{ext\,P}$, $R_{ext\,N}$ and $R_{ext\,C}$ inputs with the use of external resistors. Each Schmitt trigger operates independently offering both true (O_A, O_B) and complementary ($\overline{Z}_A$, $\overline{Z}_B$) outputs. $O_{\overline{A \oplus B}}$ provides the EXCLUSIVE-NOR function for inputs I_A and I_B. A LOW on the output enable input (EO) forces $\overline{Z}_A$ and $\overline{Z}_B$ to assume a high impedance OFF-state independent of all other input conditions.





PINNING

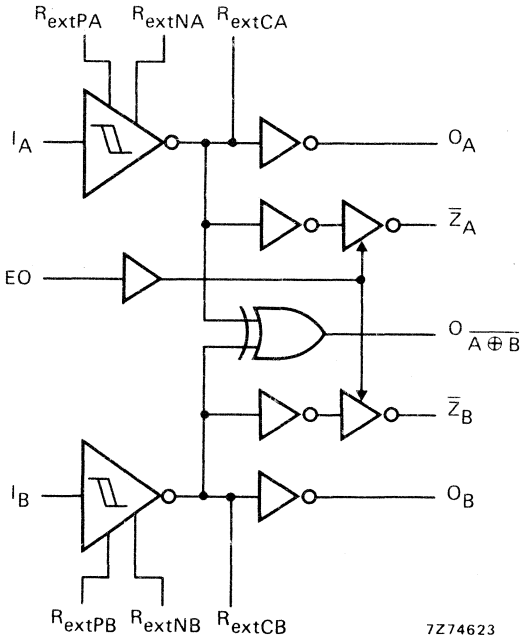
I_A, I_B	Schmitt trigger inputs
EO	output enable input
$R_{ext\,PA}$, $R_{ext\,PB}$	positive external resistor pins
$R_{ext\,NA}$, $R_{ext\,NB}$	negative external resistor pins
$R_{ext\,CA}$, $R_{ext\,CB}$	common external resistor pins
O_A, O_B	true outputs
$\overline{Z}_A$, $\overline{Z}_B$	complementary outputs
$O_{\overline{A \oplus B}}$	EXCLUSIVE-NOR output

HEF4583BP: 16-lead DIL; plastic (SOT-38Z).
HEF4583BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

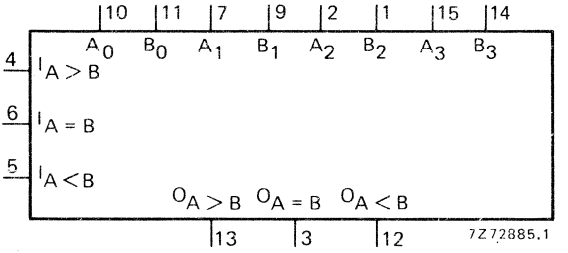
inputs			outputs				
I_A	I_B	EO	O_A	$\overline{Z}_A$	O_B	$\overline{Z}_B$	$O_{\overline{A \oplus B}}$
L	L	L	L	Z	L	Z	L
L	L	H	L	H	L	H	L
L	H	L	L	Z	H	Z	H
L	H	H	L	H	H	L	H
H	L	L	H	Z	L	Z	H
H	L	H	H	L	L	H	H
H	H	L	H	Z	H	Z	L
H	H	H	H	L	H	L	L

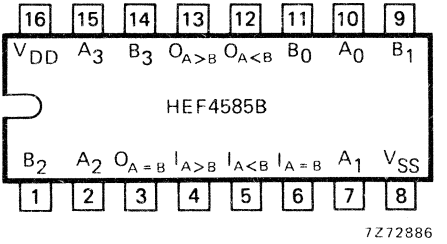
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
Z = high impedance OFF-state

4-BIT MAGNITUDE COMPARATOR

The HEF4585B is a 4-bit magnitude comparator which compares two 4-bit words (A, B), each word having four parallel inputs (A_0 to A_3 and B_0 to B_3); A_3 and B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three outputs are provided: A greater than B ($O_{A>B}$), A less than B ($O_{A<B}$), A equal to B ($O_{A=B}$). Three expander inputs ($I_{A>B}$, $I_{A<B}$ and $I_{A=B}$), allow cascading without external gates. For proper compare operation the expander inputs to the least significant position must be connected as follows: $I_{A=B} = I_{A>B}$ = HIGH, $I_{A<B}$ = LOW. For serial (ripple) expansion, the $O_{A<B}$ and $O_{A=B}$ outputs are connected respectively to the $I_{A<B}$ and $I_{A=B}$ inputs of the next most significant comparator.

The function table on page 3 describes the operation of the device under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a serial expansion scheme. The lower 2 lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.



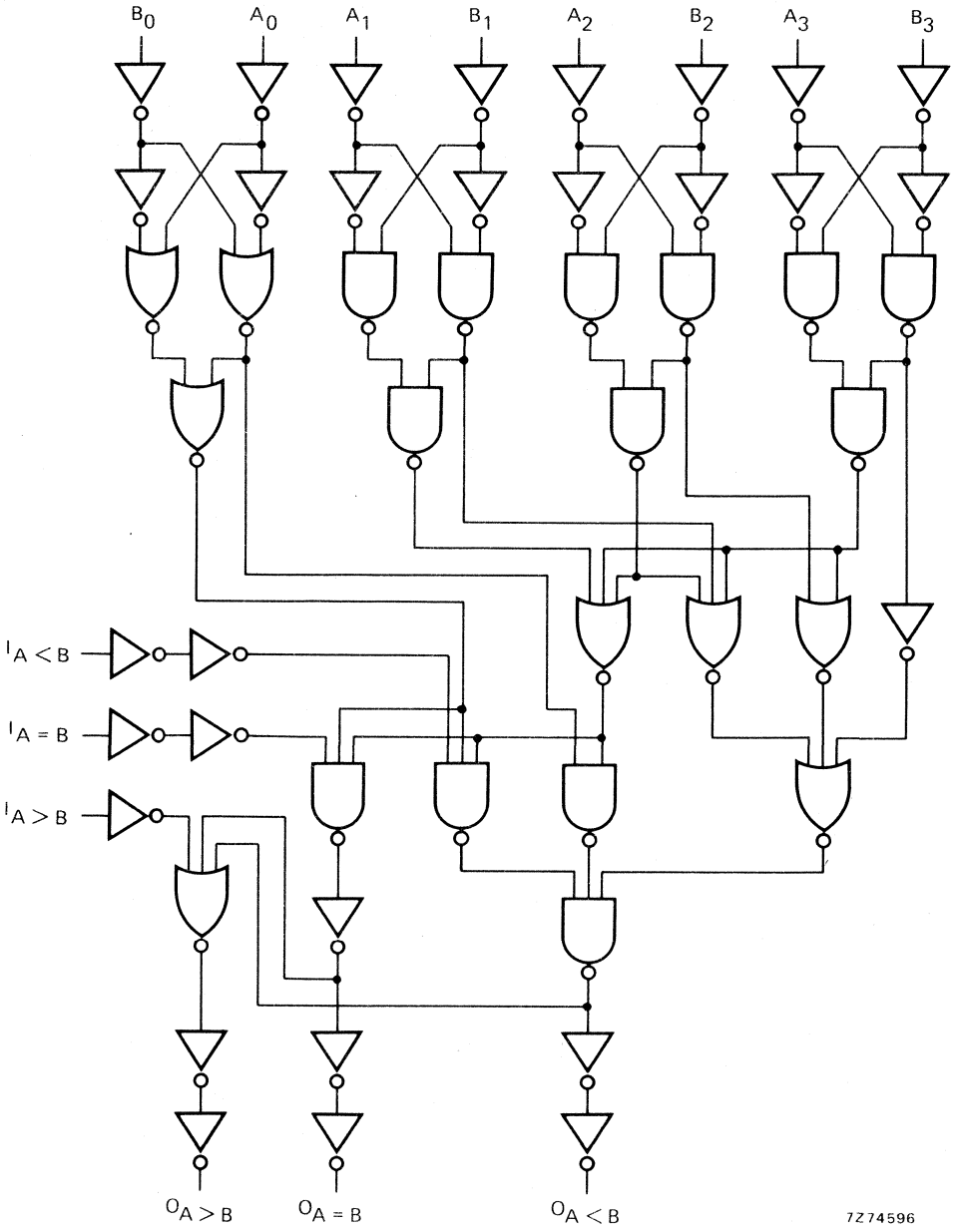


HEF4585BP: 16-lead DIL; plastic (SOT-38Z).
HEF4585BD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



PINNING

A_0 to A_3	word A parallel inputs	$O_{A>B}$	A greater than B output
B_0 to B_3	word B parallel inputs	$O_{A<B}$	A less than B output
$I_{A>B}$, $I_{A<B}$, $I_{A=B}$	expander inputs	$O_{A=B}$	A equal to B output

FUNCTION TABLE

comparing inputs				cascading inputs			outputs		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3 > B_3$	X	X	X	H	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	H	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	H	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	H	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	H	H	L	H	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	L	L	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
A_n, B_n → O_n	5			150	300 ns	123 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			140	280 ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
I_n → O_n	5			95	190 ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	75 ns	29 ns + (0,23 ns/pF) C_L
	15			30	55 ns	22 ns + (0,16 ns/pF) C_L
	5			90	180 ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	75 ns	24 ns + (0,23 ns/pF) C_L
	15			25	55 ns	17 ns + (0,16 ns/pF) C_L

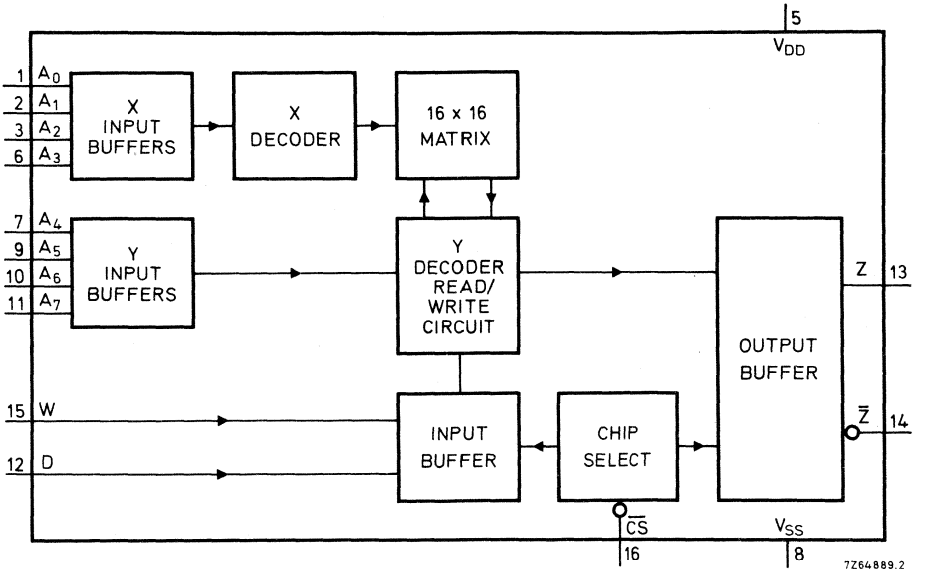
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$1900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$5400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

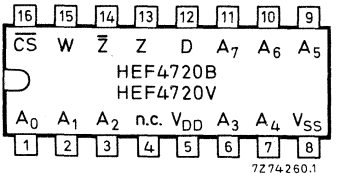
256-BIT, 1-BIT PER WORD RANDOM ACCESS MEMORIES

The HEF4720B and HEF4720V are 256-bit, 1-bit per word random access memories with 3-state outputs. The memories are fully decoded and completely static.

Recommended supply voltage range for HEF4720B is 3 to 15 V and for HEF4720V is 4,5 to 12,5 V.

The use of LOCMOS gives the added advantage of very low stand-by power. The circuits can be directly interfaced with standard bipolar devices (TTL) without using special interface circuits. The memory operates from a single power supply. The separate chip select input ($\overline{CS}$) allows simple memory expansion when the outputs are wire-ORed. If $\overline{CS}$ is HIGH, the outputs are floating and no new information can be written into the memory. The signal at Z has the same polarity as the data input D, while the signal at $\overline{Z}$ is the complement of the signal at Z. The write control W must be HIGH for writing into the memory.





HEF4720BP; HEF4720VP: 16-lead DIL; plastic (SOT-38Z).
HEF4720BD; HEF4720VD: 16-lead DIL; ceramic (SOT-74).

FAMILY DATA: see Family Specifications. **I_{DD} LIMITS category LSI:** see page 2.

FUNCTION TABLE

$\overline{CS}$	W	Z	$\overline{Z}$	mode
L	H	data written into memory	complement of data written into memory	write
L	L	data written into memory	complement of data written into memory	read
H	X	high impedance	high impedance	inhibit

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

PINNING

$\overline{CS}$	chip select input (active LOW)
W	write enable input
D	data input
A_0 to A_7	address inputs
Z	3-state output (active HIGH)
$\overline{Z}$	3-state output (active LOW)

SUPPLY VOLTAGE

	rating	recommended operating	
HEF4720B	−0,5 to 18	3,0 to 15,0	V
HEF4720V	−0,5 to 18	4,5 to 12,5	V

The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4720V, because of its lower supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current LOW	4,75	0,4	I_{OL}	2,4		2		1,6		mA
	10	0,5		4,8		4		3,2		mA
	15	1,5		10,0		10		7,5		mA
Quiescent device current	5		I_{DD}		25		25		200	μA
	10				50		50		400	μA
	15				100		100		800	μA
Input leakage current HEF4720V	10		$\pm I_{IN}$		0,3		0,3		1	μA
Input leakage current HEF4720B	15		$\pm I_{IN}$		0,3		0,3		1	μA

A.C. CHARACTERISTICS

	V_{DD} V	symbol	min	typ	max		
Output capacitance	5	C_Z		5		pF	
	10			5		pF	
	15			5		pF	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

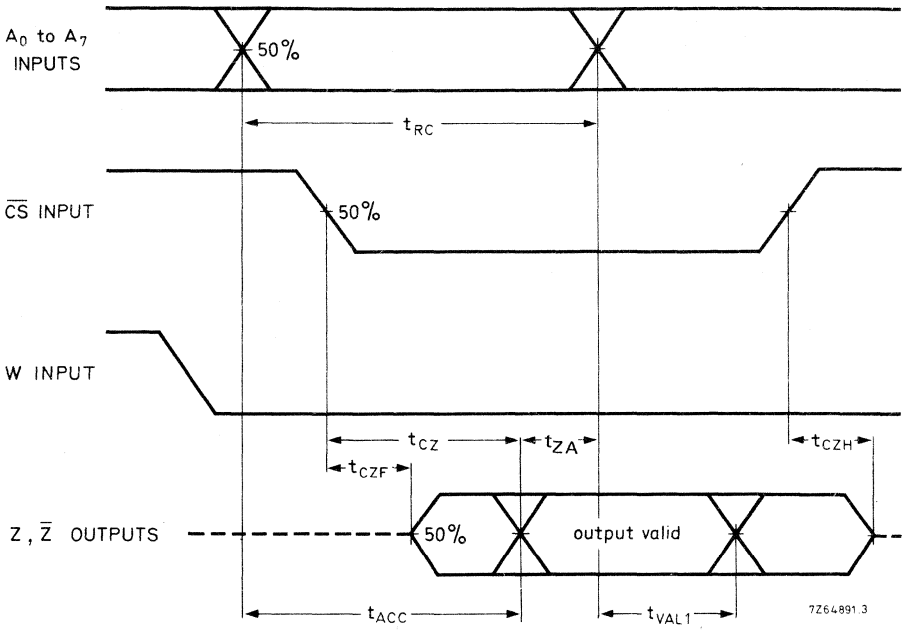
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Read cycle							
Read access time	5	t_{ACC}		320	580	ns	292 ns + (0,55 ns/pF) C_L
	10			130	220	ns	118 ns + (0,23 ns/pF) C_L
	15			100	160	ns	92 ns + (0,16 ns/pF) C_L
Chip select to output time	5	t_{CZ}			180	ns	
	10				70	ns	
	15				50	ns	
Address hold time	5	t_{ZA}	0			ns	
	10		0			ns	
	15		0			ns	
Output hold time with respect to address input	5	t_{VAL1}	60	170		ns	142 ns + (0,55 ns/pF) C_L
	10		20	50		ns	38 ns + (0,23 ns/pF) C_L
	15		15	40		ns	32 ns + (0,16 ns/pF) C_L
Output hold time with respect to chip select input	5	t_{CZH}			130	ns	
	10				70	ns	
	15				60	ns	
Output floating time with respect to chip select input	5	t_{CZF}	0			ns	
	10		0			ns	
	15		0			ns	
Read cycle time	5	t_{RC}	580			ns	
	10		220			ns	
	15		160			ns	
Transition times LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
	10			30	60	ns	9 ns + (0,42 ns/pF) C_L
	15			20	40	ns	6 ns + (0,28 ns/pF) C_L
HIGH to LOW	5	t_{THL}		40	80	ns	14 ns + (0,52 ns/pF) C_L
	10			22	40	ns	11 ns + (0,22 ns/pF) C_L
	15			15	30	ns	7 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

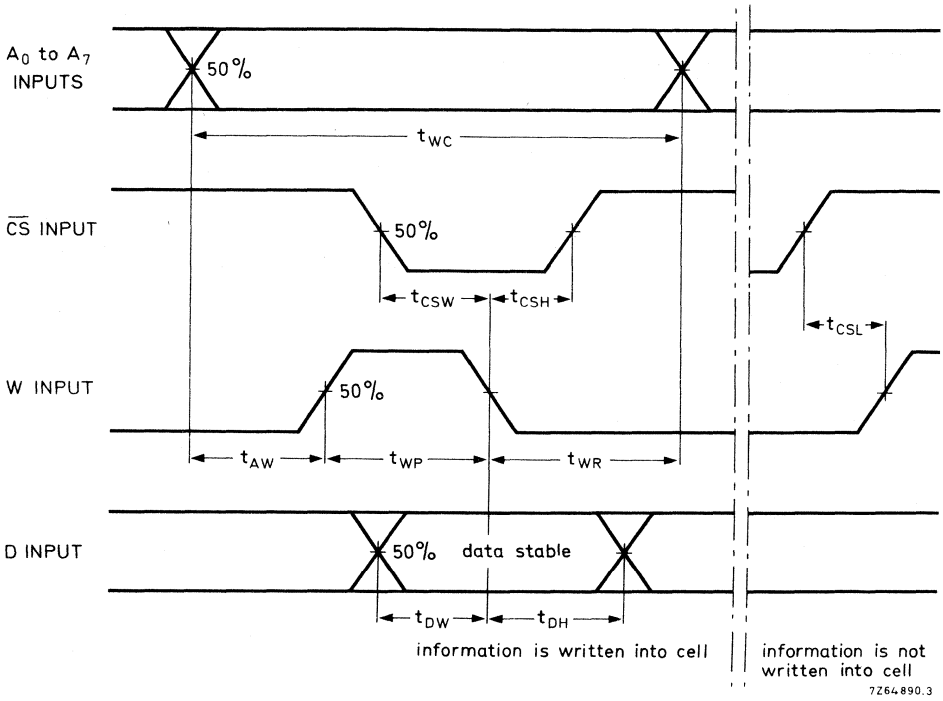
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Write cycle						
Write cycle time	5	t_{WC}	580			ns
	10		220			ns
	15		160			ns
Address to write set-up time	5	t_{AW}	110			ns
	10		50			ns
	15		50			ns
Write pulse width	5	t_{WP}	370		10 000	ns
	10		130		10 000	ns
	15		80		10 000	ns
Write recovery time	5	t_{WR}	100			ns
	10		40			ns
	15		30			ns
Data set-up time	5	t_{DW}	250			ns
	10		100			ns
	15		80			ns
Data hold time	5	t_{DH}	100			ns
	10		30			ns
	15		20			ns
Chip select set-up time with respect to write pulse	5	t_{CSW}	370			ns
	10		130			ns
	15		80			ns
Chip select hold time with respect to write pulse	5	t_{CSH}	0			ns
	10		0			ns
	15		0			ns
Chip select lead time over write pulse to prevent writing	5	t_{CSL}	0			ns
	10		0			ns
	15		0			ns
Read-modify-write cycle						
Read enable hold time	5	t_{RH}	0			ns
	10		0			ns
	15		0			ns
Output hold time with respect to write pulse	5	t_{VAL2}	60			ns
	10		20			ns
	15		15			ns
Read-modify-write cycle time	5	t_{RWC}	1050			ns
	10		390			ns
	15		270			ns

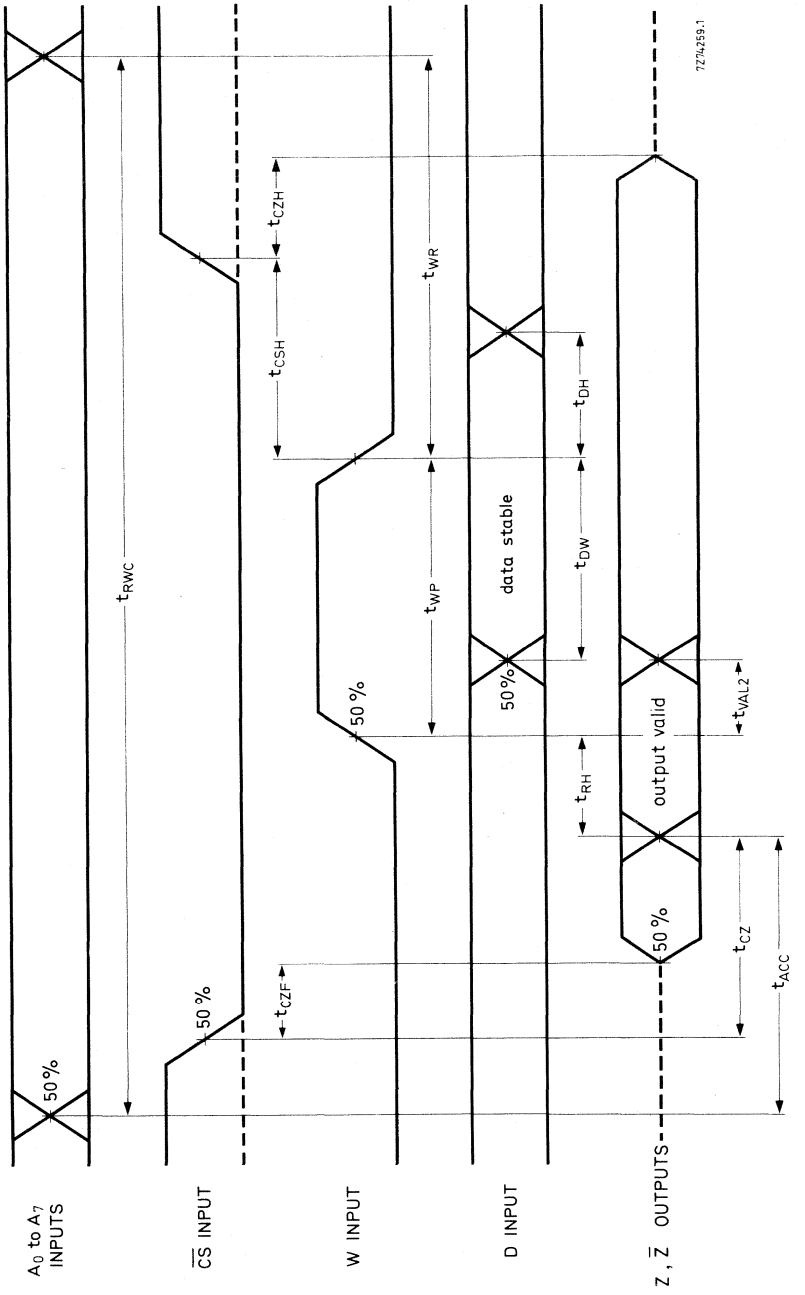
READ CYCLE TIMING DIAGRAM



WRITE CYCLE TIMING DIAGRAM



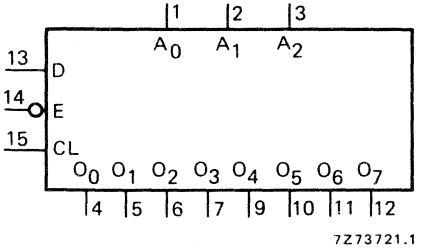
READ-MODIFY-WRITE CYCLE TIMING DIAGRAM



8-BIT ADDRESSABLE LATCH

The HEF4724B is an 8-bit addressable latch with three address inputs (A_0 to A_2), a data input (D), an active LOW enable input ($\overline{E}$), an active HIGH clear input (CL), and eight parallel latch outputs (O_0 to O_7).

When $\overline{E}$ and CL are HIGH, all outputs (O_0 to O_7) are LOW. Eight-channel demultiplexing or active HIGH 1-of-8 decoding with output enable operation occurs when CL is HIGH and $\overline{E}$ is LOW. When CL and $\overline{E}$ are LOW, the selected output (O_0 to O_7; determined by A_0 to A_2) follows D. When $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = CL = LOW), changing more than one bit of A_0 to A_2 could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = HIGH, CL = LOW).



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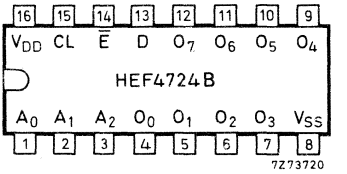


7Z73720

HEF4724BP : 16-lead DIL; plastic (SOT-38Z).
HEF4724BD: 16-lead DIL; ceramic (SOT-74).

PINNING

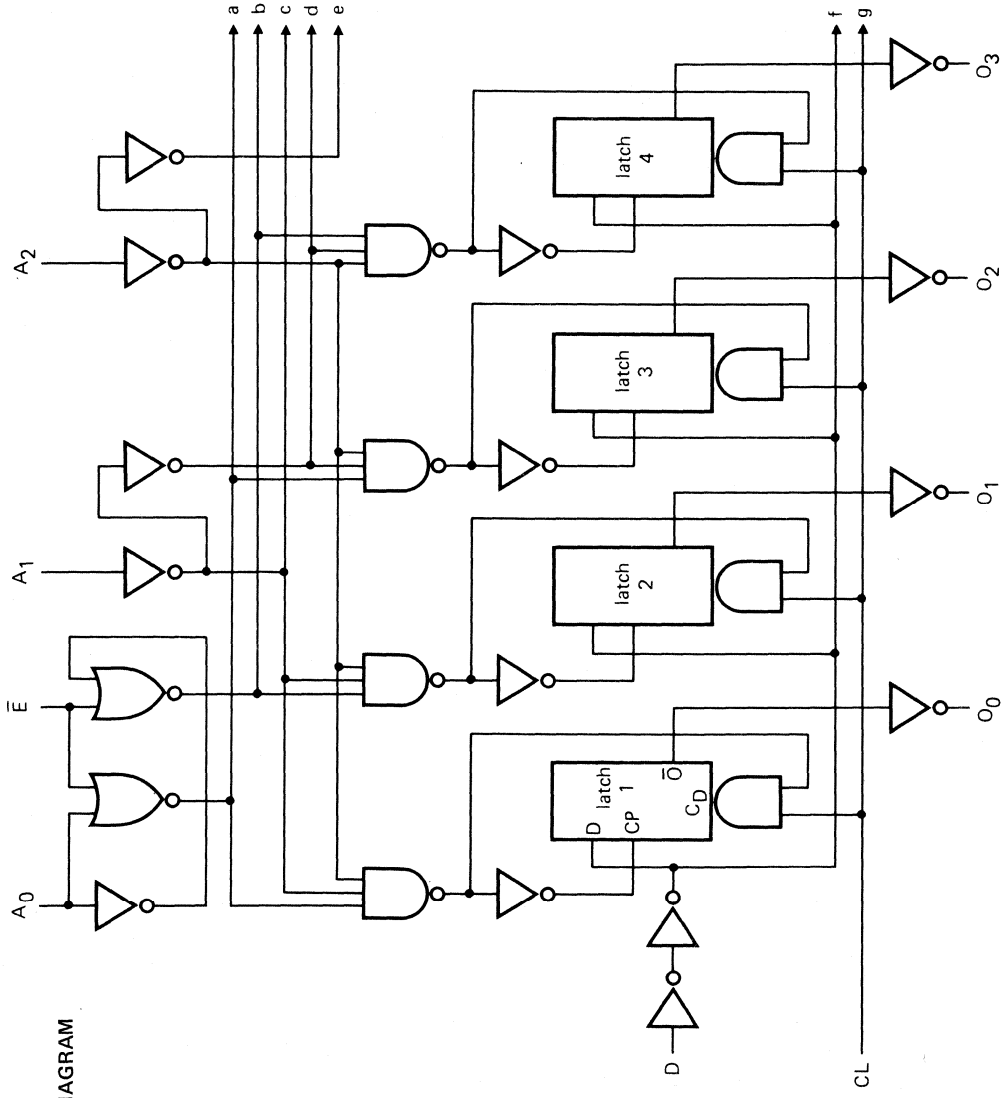
A_0 to A_2	address inputs
D	data input
$\overline{E}$	enable input (active LOW)
CL	clear input (active HIGH)
O_0 to O_7	parallel latch outputs

FAMILY DATA

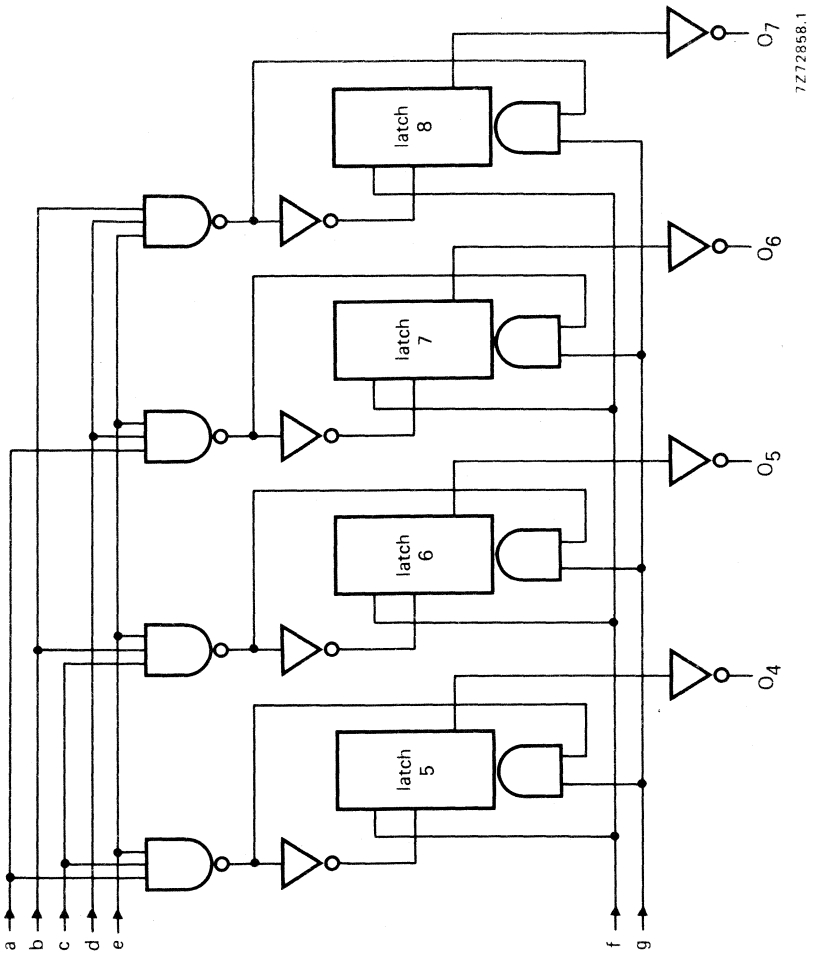
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)



MODE SELECTION

$\overline{E}$	CL	mode
L	L	addressable latch
H	L	memory
L	H	active HIGH 8-channel demultiplexer
H	H	clear

FUNCTION TABLE

CL	$\overline{E}$	D	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	mode
H	H	X	X	X	X	L	L	L	L	L	L	L	L	clear
H	L	D_1	L	L	L	D_1	L	L	L	L	L	L	L	demultiplexer; unaddressed latch is cleared
H	L	D_1	H	L	L	L	D_1	L	L	L	L	L	L	
H	L	D_1	L	H	L	L	L	D_1	L	L	L	L	L	
H	L	D_1	H	H	L	L	L	L	D_1	L	L	L	L	
H	L	D_1	L	L	H	L	L	L	L	D_1	L	L	L	
H	L	D_1	H	L	H	L	L	L	L	L	D_1	L	L	
H	L	D_1	L	H	H	L	L	L	L	L	L	D_1	L	
H	L	D_1	H	H	H	L	L	L	L	L	L	L	D_1	
L	H	X	X	X	X	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	memory
L	L	D_1	L	L	L	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	addressable latch; unaddressed latch holds previous state
L	L	D_1	H	L	L	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	L	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	H	L	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	L	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	O_{n-1}	
L	L	D_1	H	L	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	O_{n-1}	
L	L	D_1	L	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	O_{n-1}	
L	L	D_1	H	H	H	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	O_{n-1}	D_1	

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
O_{n-1} = state before the positive transition of $\overline{E}$
D_1 = either HIGH or LOW

A.C. CHARACTERISTICS

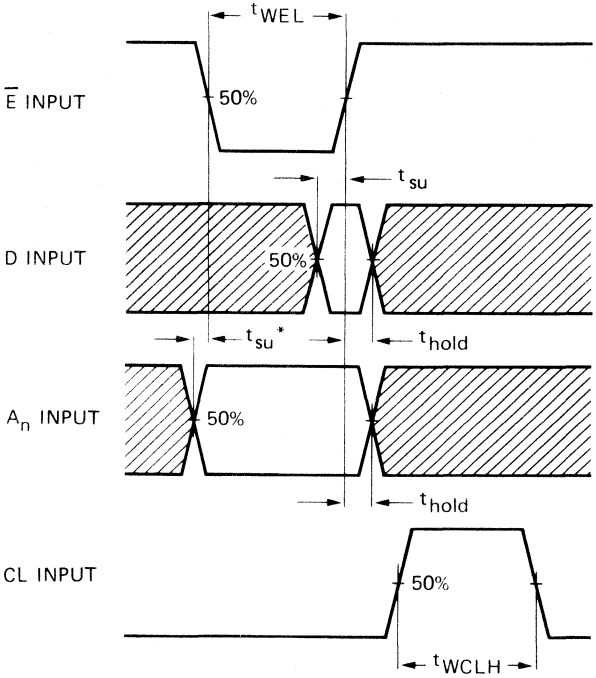
V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$3700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$10\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$\overline{E} \rightarrow O_n$	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	195	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$D \rightarrow O_n$	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
	5			85	170	ns	58 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	75	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
$A_n \rightarrow O_n$	5			110	225	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	190	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	55	ns	22 ns + (0,16 ns/pF) C_L
$CL \rightarrow O_n$	5			85	165	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Set-up times	5		40	20		ns	
$D \rightarrow \overline{E}$	10	t_{su}	15	5		ns	
	15		10	0		ns	
	5		40	20		ns	
$A_n \rightarrow \overline{E}$	10	t_{su}	20	10		ns	
	15		15	5		ns	
Hold times	5		20	0		ns	
$D \rightarrow \overline{E}$	10	t_{hold}	15	5		ns	
	15		15	5		ns	see also waveforms on page 6
	5		50	25		ns	
$A_n \rightarrow \overline{E}$	10	t_{hold}	20	10		ns	
	15		15	5		ns	
Minimum $\overline{E}$	5		75	35		ns	
pulse width; LOW	10	t_{WEL}	30	15		ns	
	15		20	10		ns	
Minimum CL	5		70	35		ns	
pulse width; HIGH	10	t_{WCLH}	30	15		ns	
	15		20	10		ns	



Waveforms showing minimum $\overline{E}$ and CL pulse widths, set-up times, hold times. Set-up and hold times are shown as positive values but may be specified as negative values.

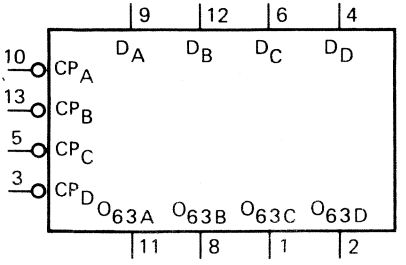
* The address to enable set-up time is the time before the HIGH to LOW enable transition that the address must be stable so that the correct latch is addressed and the other latches are not affected.

QUADRUPLE 64-BIT STATIC SHIFT REGISTER

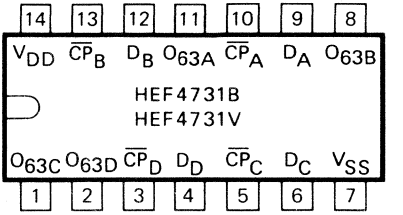
The HEF4731B and HEF4731V are quadruple 64-bit static shift registers each with separate serial data inputs (D_A to D_D), clock inputs ($\overline{CP}_A$ to $\overline{CP}_D$) and data outputs (O_{63A} to O_{63D}) from the 64th register position.

Recommended supply voltage range for HEF4731B is 3 to 15 V and for HEF4731V is 4,5 to 12,5 V.

The data is accepted when the clock is HIGH while the output changes on the HIGH to LOW transition of the clock. Low impedance outputs are provided for direct interface to TTL.



7Z74633



7Z74631

HEF4731BP ; HEF4731VP : 14-lead DIL; plastic (SOT-27).
HEF4731BD; HEF4731VD: 14-lead DIL; ceramic (SOT-73).

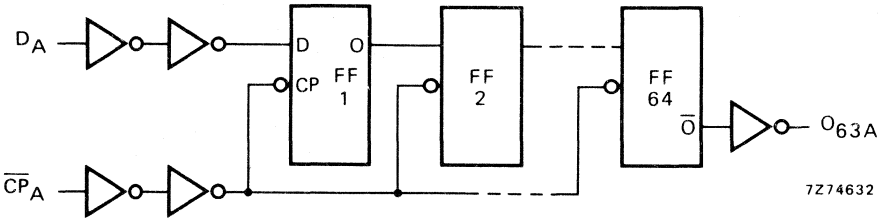
SUPPLY VOLTAGE

	rating	recommended operating	
HEF4731B	−0,5 to 18	3,0 to 15,0	V
HEF4731V	−0,5 to 18	4,5 to 12,5	V

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 2

LOGIC DIAGRAM (one register)



The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4731V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	V_{OH} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
	5		2,5		3		2,5		2,0		mA
Output current HIGH	5		4,6	$-I_{OH}$	1		0,85		0,65		mA
	10		9,5		3		2,5		2,0		mA
	15		13,5		10		8,5		6,5		mA
Output current LOW	4,75	0,4			2,7		2,3		1,8		mA
	10	0,5		I_{OL}	9,5		8,0		6,3		mA
	15	1,5			24,0		20,0		16,0		mA
Quiescent device current	5					50		50		375	μA
	10			I_{DD}		100		100		750	μA
	15					200		200		1500	μA

A.C. CHARACTERISTICS

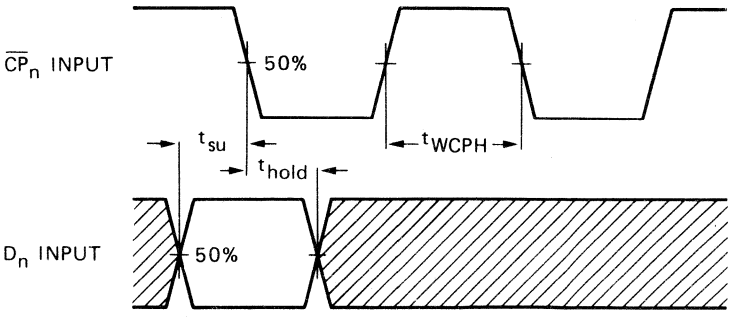
V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$12\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$50\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$130\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
$\overline{CP} \rightarrow O_{63}$	5			240	ns	227 ns + (0,26 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	ns	77 ns + (0,16 ns/pF) C_L
	15			60	ns	54 ns + (0,11 ns/pF) C_L
	5			220	ns	198 ns + (0,45 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		80	ns	71 ns + (0,19 ns/pF) C_L
	15			55	ns	49 ns + (0,13 ns/pF) C_L
Transition times	5			35	ns	15 ns + (0,40 ns/pF) C_L
HIGH to LOW	10	t_{THL}		17	ns	8 ns + (0,18 ns/pF) C_L
	15			13	ns	7 ns + (0,13 ns/pF) C_L
	5			50	ns	18 ns + (0,65 ns/pF) C_L
LOW to HIGH	10	t_{TLH}		25	ns	10 ns + (0,30 ns/pF) C_L
	15			20	ns	10 ns + (0,20 ns/pF) C_L
Minimum clock	5			95	ns	
pulse width; HIGH	10	t_{WCPH}		30	ns	
	15			20	ns	
Set-up time	5			−5	ns	
D → $\overline{CP}$	10	t_{su}		0	ns	
	15			0	ns	see also waveforms below
Hold time	5			20	ns	
D → $\overline{CP}$	10	t_{hold}		10	ns	
	15			5	ns	
Maximum clock	5			5	MHz	
pulse frequency	10	f_{max}		14	MHz	
	15			20	MHz	



Waveforms showing minimum clock pulse width, set-up and hold times for D to $\overline{CP}$. Set-up and hold times are shown as positive values but may be specified as negative values.

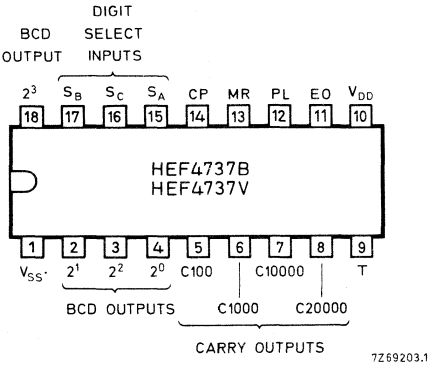
QUADRUPLE STATIC DECADE COUNTERS

The HEF4737B and HEF4737V are static quadruple decade counters for frequencies from 0 to 10 MHz. The counters are supplied with an extra overload flip-flop giving a total count capability of 19 999.

The complementary MOS structure gives the devices very low stand-by and operating dissipation. Operating from a single supply voltage all outputs can drive one normal TTL input without interface circuitry under all specified operating conditions.

The BCD digit outputs are complementary MOS 3-state outputs enabling very easy cascading of devices. The counters are supplied with asynchronous reset and preset to 19 999 facilities making them suitable for counter and time base applications. All carry signals are available except from the first decade.

Recommended supply voltage range for HEF4737B is 3 to 15 V and for HEF4737V is 4,5 to 12,5 V.



HEF4737BP; HEF4737VP: 18-lead DIL; plastic (SOT-102A).

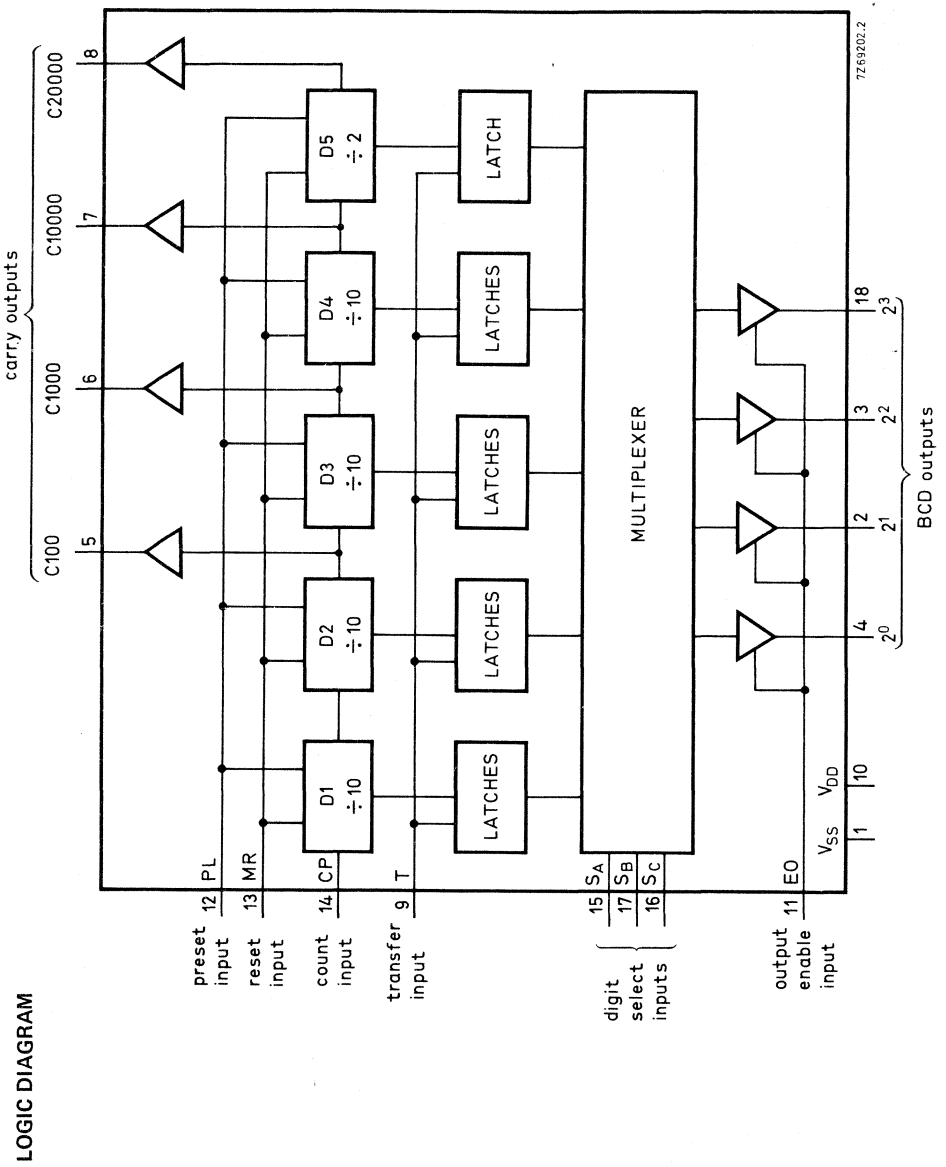
SUPPLY VOLTAGE

	rating	recommended operating	
HEF4737B	−0,5 to 18	3,0 to 15,0	V
HEF4737V	−0,5 to 18	4,5 to 12,5	V

FAMILY DATA: see Family Specifications

I_{DD} LIMITS category LSI: see page 6

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Input signals

Count input

The signal to be counted is applied to this input. A LOW to HIGH transition at this input increments the contents of the counter by 1.

Reset input

This is an asynchronous reset. A HIGH level applied to this input will reset the counter to zero independent of the level at the count input.

Preset input

This is an asynchronous preset. A HIGH level applied to this input will preset the counter to 19 999 independent of the level at the count input.

Transfer input

A HIGH level applied to this input allows the information held by the counter to pass to the latches.

Output enable input

A HIGH level at this input enables the BCD outputs and information can be read out of the latches using the multiplexer. A LOW level at this input disables the BCD outputs making them floating.

Digit select inputs

S_A	S_B	S_C	
L	L	L	selects D1 (LSD)
H	L	L	selects D2
L	H	L	selects D3
H	H	L	selects D4
X	X	H	selects D5 (MSD)

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

FUNCTIONAL DESCRIPTION (continued)

Output signals

Carry output C100

When the contents of the first two decades of the counter are both 9 then the C100 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first two decades are zero. C100 is LOW when the contents of the counter are: 00 099, 00 199, 00 299 etc.

Carry output C1000

When the contents of the first three decades of the counter are all 9 then the C1000 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first three decades are zero. C1000 is LOW when the contents of the counter are 00 999, 01 999, 02 999 etc.

Carry output C10 000

When the contents of the first four **decades** of the counter are all 9 then the C10 000 output becomes LOW. It remains LOW until the next LOW to HIGH transition of the count input, i.e. until the contents of the first four decades are zero. C10 000 is LOW when the contents of the counter are 09 999 and 19 999.

The carry signals C100, C1000 and C10 000 are suppressed while the preset is active. A HIGH to preset input sets the counter to 19 999 but the carry signals remain HIGH until preset input returns to LOW, when the carry inputs will also become LOW.

Carry output C20 000

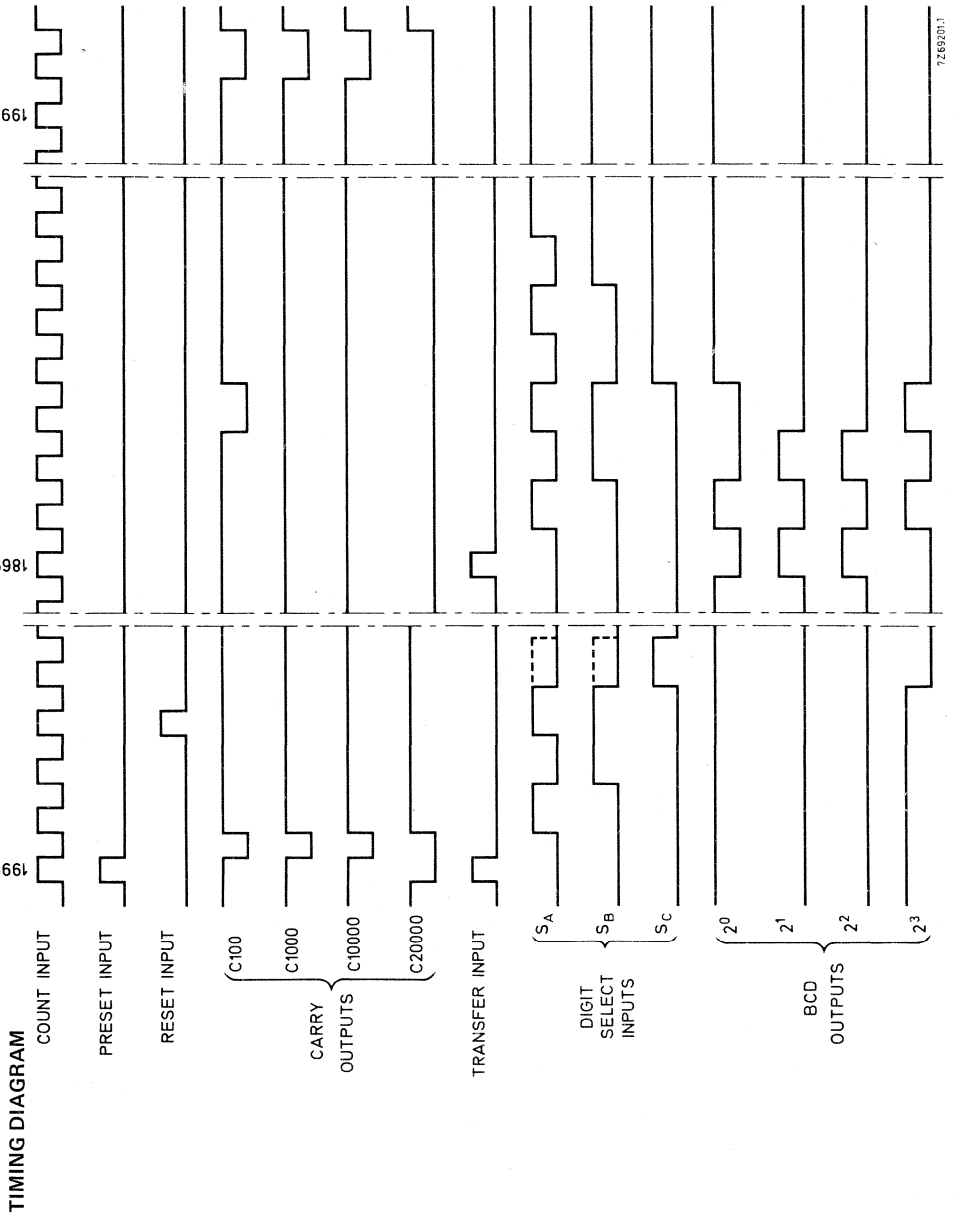
When the content of the counter is 10 000 the C20 000 output becomes LOW. It returns to HIGH when the content of the counter is zero.

Digit outputs

The digit outputs give the contents of the selected latch. The output is in the form of BCD, positive logic.

DEVELOPMENT SAMPLE DATA

TIMING DIAGRAM



The values given at V_{DD} = 15 V in the following d.c. and a.c. characteristics, are not applicable to the HEF4737V, because of its reduced supply voltage range.

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+ 25 min	+ 25 max	+ 85 min	+ 85 max	
Output current HIGH	4,75	4,25		$-I_{OH}$	0,4		0,4		0,4		mA
Output current LOW	4,75		0,4	I_{OL}	1,6		1,6		1,6		mA
Quiescent device current	5			I_{DD}		50		50		375	μA
	10					100		100		750	μA
	15					200		200		1500	μA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 15 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Count input pulse width; LOW	5	t_{WCPL}	150			ns
	10		50			ns
HIGH	5	t_{WCPH}	150			ns
	10		50			ns
Reset pulse width HIGH	5	t_{WMRH}	100			ns
	10		50			ns
Preset pulse width HIGH	5	t_{WPLH}	100			ns
	10		50			ns
Transfer pulse width HIGH	5	t_{WTH}	100			ns
	10		50			ns
Count frequency	5	f_c	3			MHz
	10		10			MHz

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 15 pF; input transition times ⩽ 20 ns

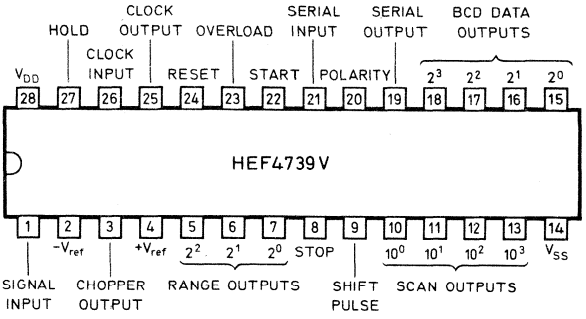
	V_{DD} V	symbol	min	typ	max	
Propagation delays						
CP → BCD	5	t_{PHL},			900	ns
	10	t_{PLH}			450	ns
CP → carry	5	t_{PHL},			750	ns
	10	t_{PLH}			350	ns
S_n → BCD	5	t_{PHL},			200	ns
	10	t_{PLH}			75	ns
T → BCD	5	t_{PHL},			400	ns
	10	t_{PLH}			200	ns
MR → BCD	5	t_{PHL},			900	ns
	10	t_{PLH}			450	ns
PL → BCD	5	t_{PHL},			500	ns
	10	t_{PLH}			250	ns
MR → carry	5	t_{PHL},			750	ns
	10	t_{PLH}			350	ns
PL → carry	5	t_{PHL},			750	ns
	10	t_{PLH}			350	ns
Transition times						
BCD outputs	5	t_{THL},			120	ns
	10	t_{TLH}			60	ns
carry outputs	5	t_{THL},			100	ns
	10	t_{TLH}			50	ns

DEVELOPMENT SAMPLE DATA

DIGITAL VOLTMETER CIRCUIT

The HEF4739V is intended for use in dual polarity digital voltmeters where the delta-modulation principle is used for analogue to digital conversion. The device contains all the digital logic of the voltmeter including the facility for automatic range selection. Each output can drive one TTL input under all specified conditions.

Recommended operating supply voltage range is 4,5 to 12,5 V (−0,5 to + 18 V as a rating).



HEF4739VP: 28-lead DIL; plastic (SOT-117).

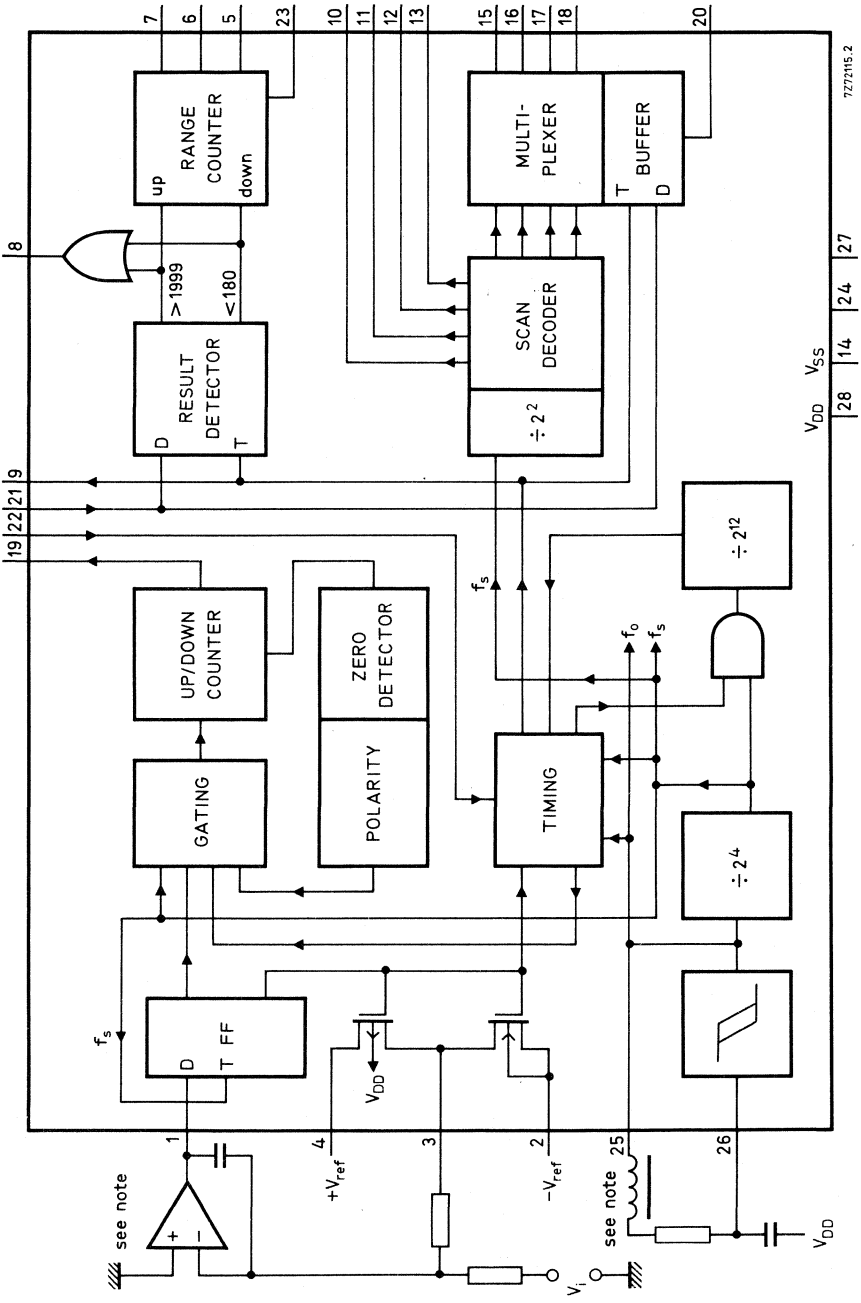
PINNING

1. Signal input
2. $-V_{ref}$
3. Chopper output
4. $+V_{ref}$
5. 2^2; range output
6. 2^1; range output
7. 2^0; range output
8. Stop output
9. Shift pulse output
10. 10^0; scan output
11. 10^1; scan output
12. 10^2; scan output
13. 10^3; scan output
14. V_{SS} (ground)
15. 2^0; BCD data output
16. 2^1; BCD data output
17. 2^2; BCD data output
18. 2^3; BCD data output
19. Serial output
20. Polarity output
21. Serial input
22. Start input
23. Overload output
24. Reset input
25. Clock output
26. Clock input
27. Data hold input
28. V_{DD} (supply voltage)

FAMILY DATA see Family Specifications

I_{DD} LIMITS category LSI see page 6

LOGIC DIAGRAM



Note: system earth not connected to V_{SS}.

FUNCTIONAL DESCRIPTION

Signal input (pin 1)

To be connected with output of an integrator.
HIGH: chopper output connected with $+V_{ref}$
LOW : chopper output connected with $-V_{ref}$

Chopper output (pin 3)

To be connected with input of an integrator.
When signal input is HIGH: chopper output is connected with $+V_{ref}$
When signal input is LOW : chopper output is connected with $-V_{ref}$

Reference inputs

$+V_{ref}$ has to be connected to the positive reference voltage of the system and $-V_{ref}$ to the negative reference voltage.

Polarity output

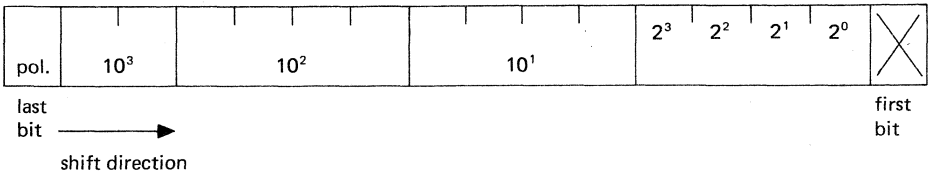
This output is HIGH if the signal input is more frequently HIGH than LOW.

Clock input/clock output

The clock frequency is determined by external components. The clock input can be used as an input if an external clock is applied. The clock frequency (f_o) is 16 times the sample frequency (f_s) and the measuring time is 65 536 clock pulses.

Serial input/serial output/shift pulse output

The serial input and serial output pins should be externally connected together. Between two measurements a train of 16 pulses appear at the shift pulse output. This pulse train is used internally to shift the information from the up/down counter to the buffer. The serial output is the output of the up/down counter and serial input is the input to the buffer.
The 16-bit serial information is as follows:



From these 16 bits the first bit should be neglected and the last bit gives the polarity.

Start input/stop output

The built-in automatic ranging circuit will select a higher range if the result is greater than 1999 and a lower range if the result is less than 180. A change in range will be indicated by a LOW on the stop output. In order to allow the external ranging circuitry to respond to a change in range the next measuring period will be delayed until the start input has been HIGH for at least 16 clock pulses.

Range outputs/overload output

The range outputs present in binary form the state of the range selector. The overload output becomes HIGH when the measuring result is greater than 1999 independent of the selected range.

FUNCTIONAL DESCRIPTION (continued)

BCD data outputs

These outputs show the contents of the selected digit of the buffer register in BCD code.

Scan outputs

These outputs show at each moment which digit of the buffer has been selected. The selected output is HIGH: scan sequence $10^3 - 10^2 - 10^1 - 10^0$. The scan pulses are separated by one clock pulse (interdigit blanking).

Reset input/data hold input (see function table below)

When the reset input has been LOW for at least 32 clock pulses the circuit is completely reset. The ranging is then in the lowest position and the 10^3 digit is selected. After reset the next measuring period starts. When having data hold mode the last measuring result is maintained.

FUNCTION TABLE

reset	hold	function
L	L	test mode *
L	H	reset
H	L	data hold
H	H	normal operation

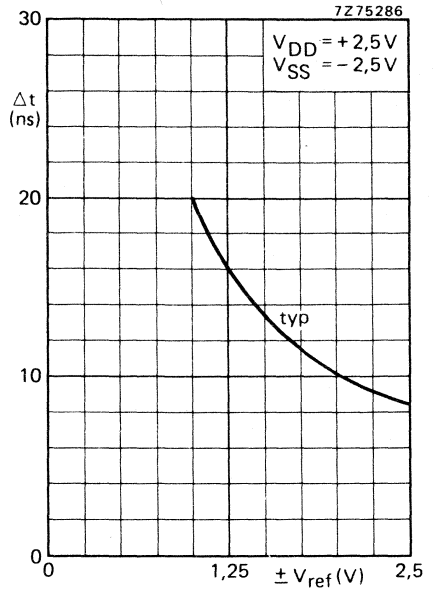
* Used for final testing in the factory.

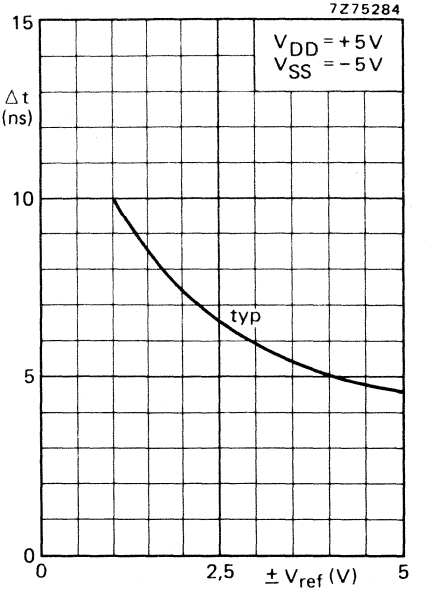
A.C. CHARACTERISTICS

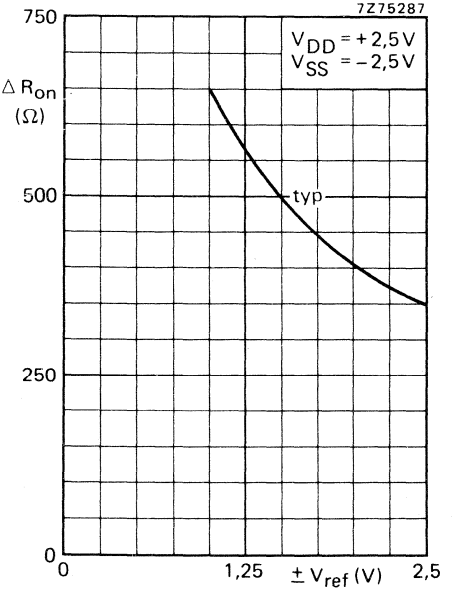
T_{amb} = 25 °C; input transition time $\leqslant$ 20 ns; input voltage swing = $V_{SS} - V_{DD}$; output load capacitance = 15 pF; all times referred to 50% voltage swing.

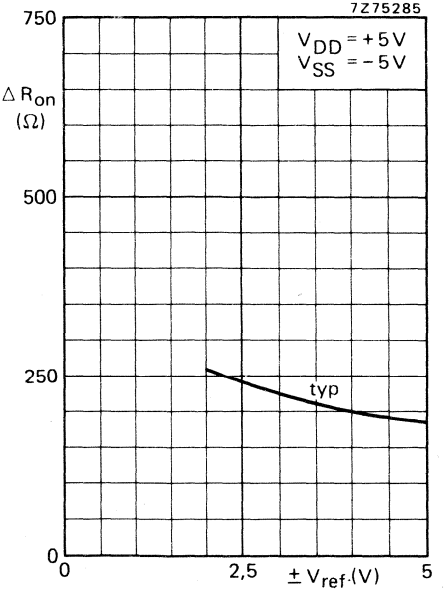
	symbol	min	typ	max		conditions and references	
						V_{DD} V	
Clock input frequency	f_{max}	1	2	–	MHz	5	
		2	4	–	MHz	10	
Switching speed unbalance of chopper	Δt	–	10	50	ns		V_{DD} = +2,5 V; V_{SS} = −2,5 V; V_{ref} = ±2048 mV
		–	5	25	ns		V_{DD} = +5 V; V_{SS} = −5 V; V_{ref} = ±4096 mV
ON resistance unbalance	ΔR_{on}	–	400	–	Ω	5	V_{DD} = +2,5 V; V_{SS} = −2,5 V; V_{ref} = ±2048 mV
		–	200	–	Ω	10	V_{DD} = +5 V; V_{SS} = −5 V; V_{ref} = ±4096 mV

DEVELOPMENT SAMPLE DATA









From the graphs above it is clear that the accuracy of the system is optimum when $\pm V_{ref}$ is as close as possible to the supply voltage.

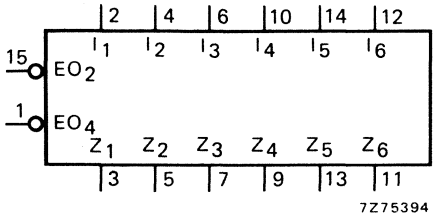
D.C. CHARACTERISTICS

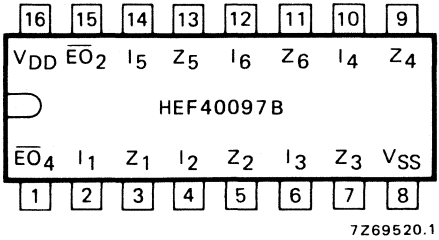
V_{SS} = 0 V

parameter	V_{DD} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	unit	conditions
Quiescent device current	5	I_{DD}	–	50	–	50	–	375	μA	all valid input combinations; $V_I = V_{SS}$ or V_{DD}
	10		–	100	–	100	–	750	μA	
Clock input voltage LOW	5	V_{IL}	–	0,2	–	0,2	–	0,2	V	
	10		–	–	–	–	–	–	V	
Clock input voltage HIGH	5	V_{IH}	4,8	–	4,8	–	4,8	–	V	
	10		–	–	–	–	–	–	V	
Reference voltage	V_{DD}	$+V_{ref}$	← min 3 max V_{DD} →						V	$+V_{ref} > -V_{ref}$
	V_{DD}	$-V_{ref}$	← min −1 max $V_{DD}-3$ →						V	
Chopper output LOW	V_{DD}	V_{CHL}	← typ $-V_{ref}$ →						V	
Chopper output HIGH	V_{DD}	V_{CHH}	← typ $+V_{ref}$ →						V	
Output (sink) current LOW	5	I_{OL}	2,4	–	2,0	–	1,6	–	mA	V_O = 0,4 V; V_I = 0 or 5 V
	10		4,8	–	4,0	–	3,2	–	mA	V_O = 0,5 V; V_I = 0 or 10 V
Output (source) current HIGH	5	I_{OH}	0,7	–	0,7	–	0,4	–	mA	V_O = 4,6 V; V_I = 0 or 5 V
	10		1,4	–	1,4	–	0,8	–	mA	V_O = 9,5 V; V_I = 0 or 10 V

3-STATE HEX NON-INVERTING BUFFER

The HEF40097B is a hex non-inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state, regardless of the other input conditions.





HEF40097BP: 16-lead DIL; plastic (SOT-38Z).
HEF40097BD: 16-lead DIL; ceramic (SOT-74).

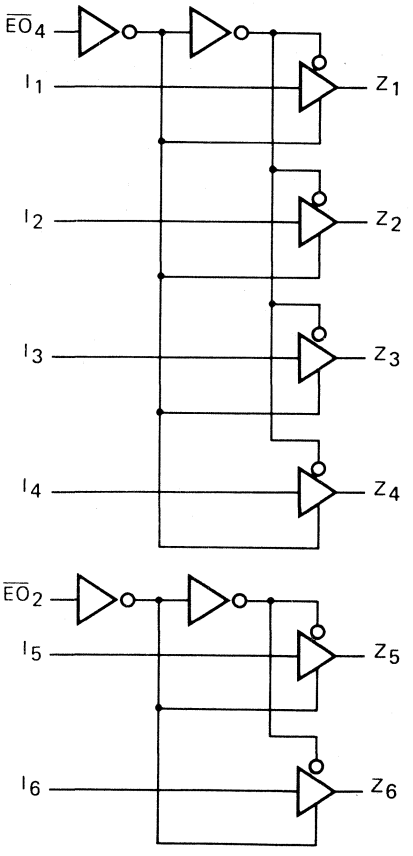
PINNING

I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
Z_1 to Z_6	buffer outputs (active HIGH)

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

LOGIC DIAGRAM



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D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current HIGH	5	4,6		$-I_{OH}$	1,2		1,0		0,8		mA
	10	9,5			3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4	I_{OL}	3,5		2,9		2,3		mA
	10		0,5		12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

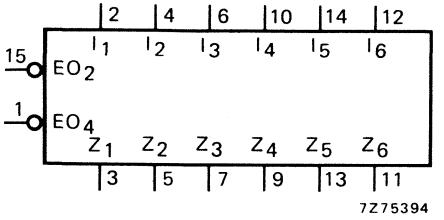
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

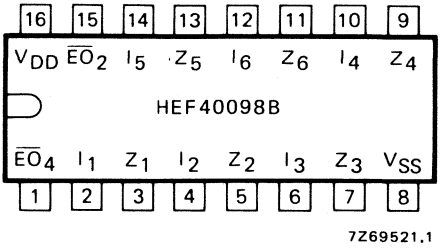
	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow Z_n$	5		70	140	ns	60 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	30	60	ns	26 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
	5		60	120	ns	45 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	25	50	ns	19 ns + (0,13 ns/pF) C_L
	15		20	40	ns	16 ns + (0,09 ns/pF) C_L
Transition times	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
Output disable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow Z_n$	5		45	95	ns	
HIGH	10	t_{PHZ}	35	70	ns	
	15		30	60	ns	
	5		60	120	ns	
LOW	10	t_{PLZ}	35	70	ns	
	15		25	55	ns	
Output enable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow Z_n$	5		75	150	ns	
HIGH	10	t_{PZH}	35	70	ns	
	15		30	60	ns	
	5		95	190	ns	
LOW	10	t_{PZL}	40	80	ns	
	15		30	65	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	5400 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	25 200 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	96 500 $f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

3-STATE HEX INVERTING BUFFER

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.





HEF40098BP : 16-lead DIL; plastic (SOT-38Z).
HEF40098BD: 16-lead DIL; ceramic (SOT-74).

PINNING

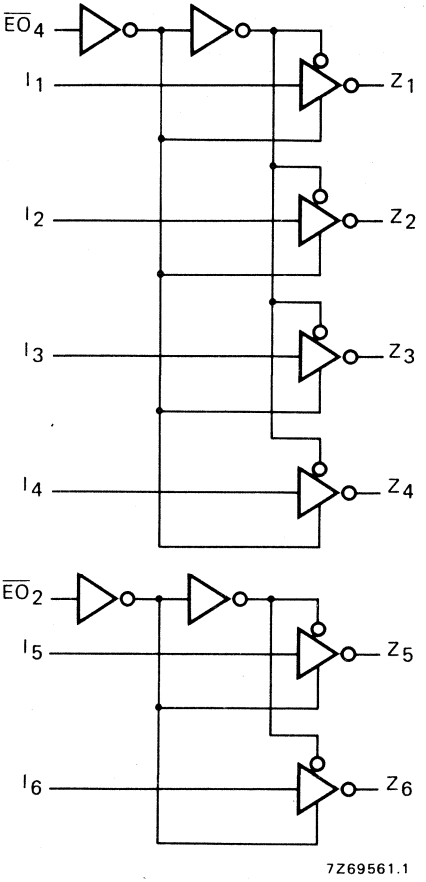
I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
Z_1 to Z_6	buffer outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category BUFFERS

see Family Specifications

LOGIC DIAGRAM



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D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min	−40 max	+25 min	+25 max	+85 min	+85 max	
Output current HIGH	5	4,6			1,2		1,0		0,8		mA
	10	9,5		$-I_{OH}$	3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4,75		0,4		3,5		2,9		2,3		mA
	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

A.C. CHARACTERISTICS

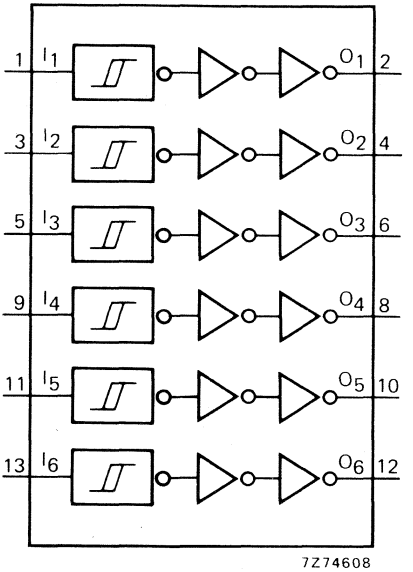
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ	max		typical extrapolation formula
Propagation delays						
$I_n \rightarrow Z_n$	5		80	160	ns	70 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	31 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
	5		65	130	ns	50 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	24 ns + (0,13 ns/pF) C_L
	15		25	50	ns	21 ns + (0,05 ns/pF) C_L
Transition times	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
Output disable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow Z_n$	5		45	85	ns	
HIGH	10	t_{PHZ}	35	65	ns	
	15		30	60	ns	
	5		65	135	ns	
LOW	10	t_{PLZ}	40	80	ns	
	15		35	70	ns	
Output enable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow Z_n$	5		70	140	ns	
HIGH	10	t_{PZH}	35	75	ns	
	15		30	65	ns	
	5		90	185	ns	
LOW	10	t_{PZL}	40	85	ns	
	15		35	70	ns	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	5000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	22 800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	
	15	81 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	

HEX SCHMITT TRIGGER

The HEF40106B performs the function of six Schmitt-trigger circuits. This device may be used for enhanced noise immunity or to 'square-up' slowly changing waveforms.



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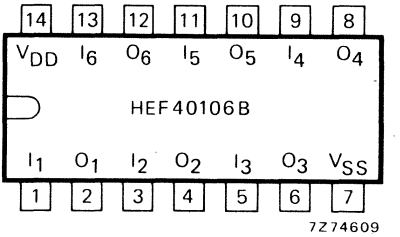

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HEF40106BP: 14-lead DIL; plastic (SOT-27).
HEF40106BD: 14-lead DIL; ceramic (SOT-73).

LOGIC DIAGRAM

Identical to the one above.

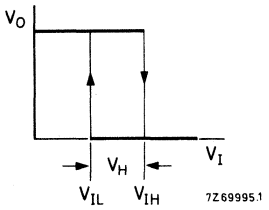
FAMILY DATA

I_{DD} LIMITS category GATES } see Family Specifications

D.C. CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	symbol	T_{amb} (°C) −40 min typ max	+ 25 min typ max	+ 85 min typ max	
Hysteresis voltage	5	V_H		0,4		V
	10			0,7		V
	15			0,9		V



Transfer characteristic

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

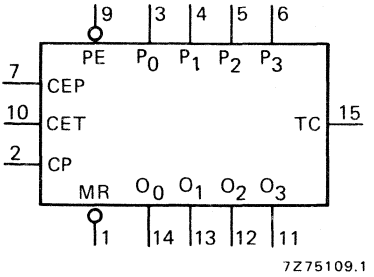
	V_{DD} V	symbol	typ	max	typical extrapolation formula
Propagation delays					
$I_n \rightarrow O_n$	5		90	ns	63 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	40	ns	29 ns + (0,23 ns/pF) C_L
	15		30	ns	22 ns + (0,16 ns/pF) C_L
	5		90	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	40	ns	29 ns + (0,23 ns/pF) C_L
	15		30	ns	22 ns + (0,16 ns/pF) C_L

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	2 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
	10	10 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
	15	30 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	C_L = load capacitance (pF)
			$\Sigma(f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

4-BIT SYNCHRONOUS DECADE COUNTER WITH ASYNCHRONOUS RESET

The HEF40160B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), an overriding asynchronous master reset ($\overline{MR}$), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{MR}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3$ = HIGH, $O_1 = O_2$ = LOW) and when CET is HIGH. A LOW on $\overline{MR}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique. CEP, CET and $\overline{PE}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.



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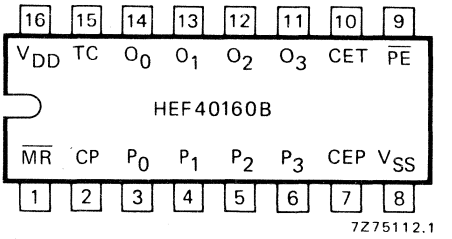

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HEF40160BP : 16-lead DIL; plastic (SOT-38Z).
HEF40160BD: 16-lead DIL; ceramic (SOT-74).

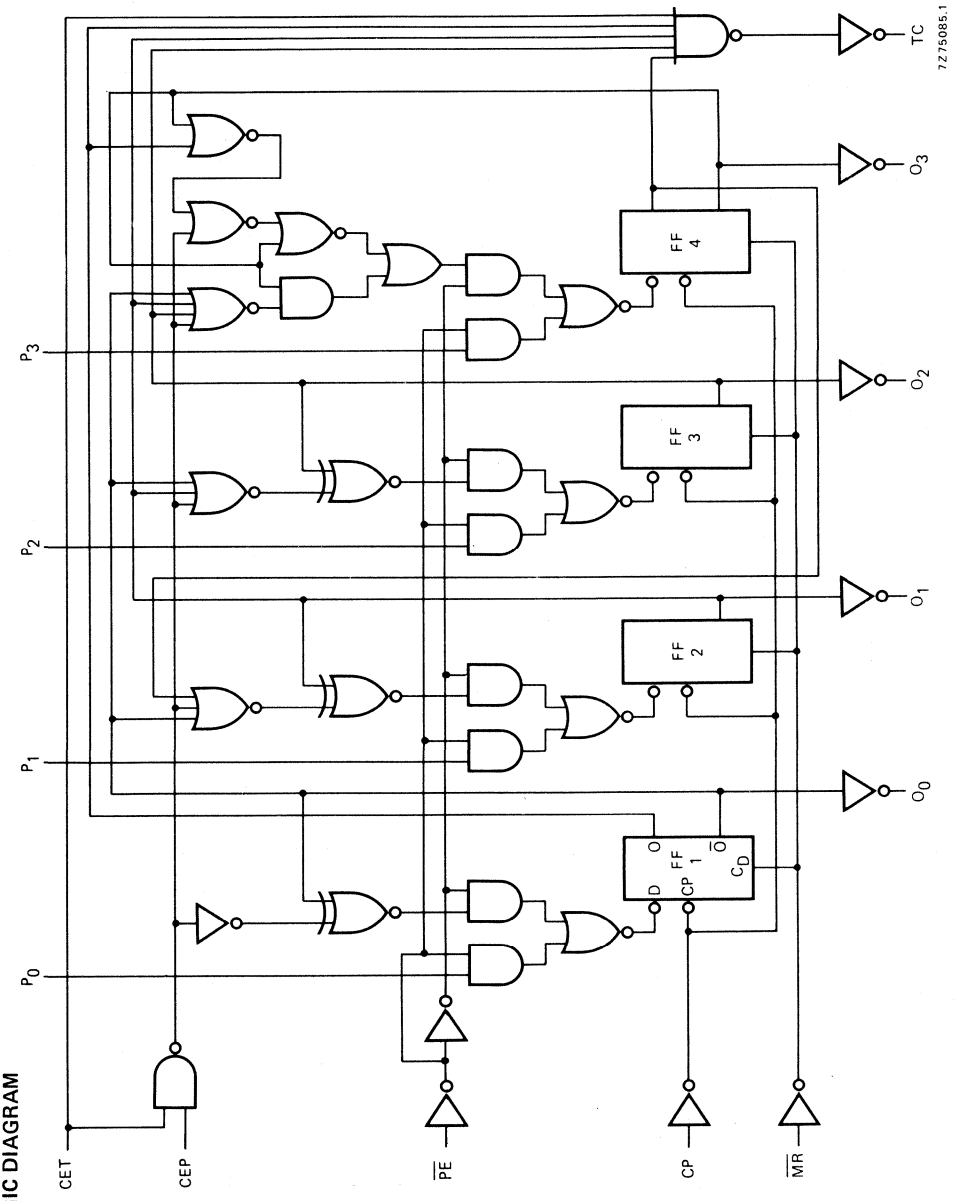
PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

FAMILY DATA

I_{DD} LIMITS category MSI | see Family Specifications

LOGIC DIAGRAM



SYNCHRONOUS MODE SELECTION

$\overline{PE}$	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

$\overline{MR}$ = HIGH

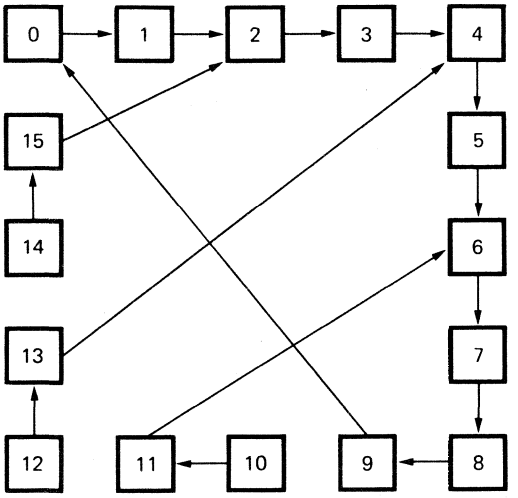
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3$

STATE DIAGRAM



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A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

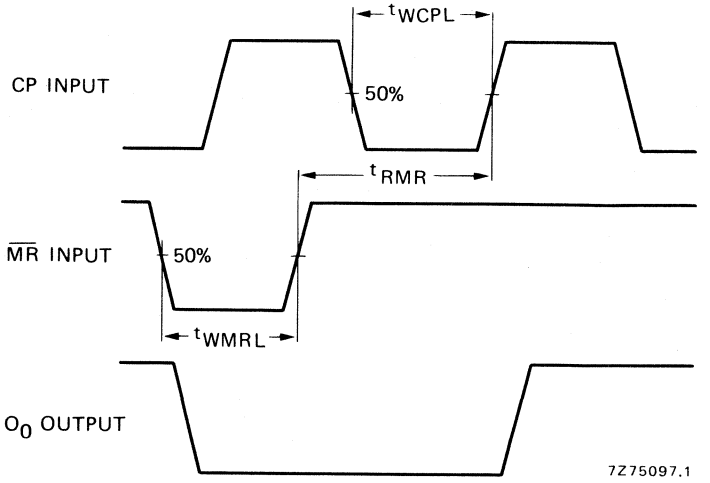
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → TC	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

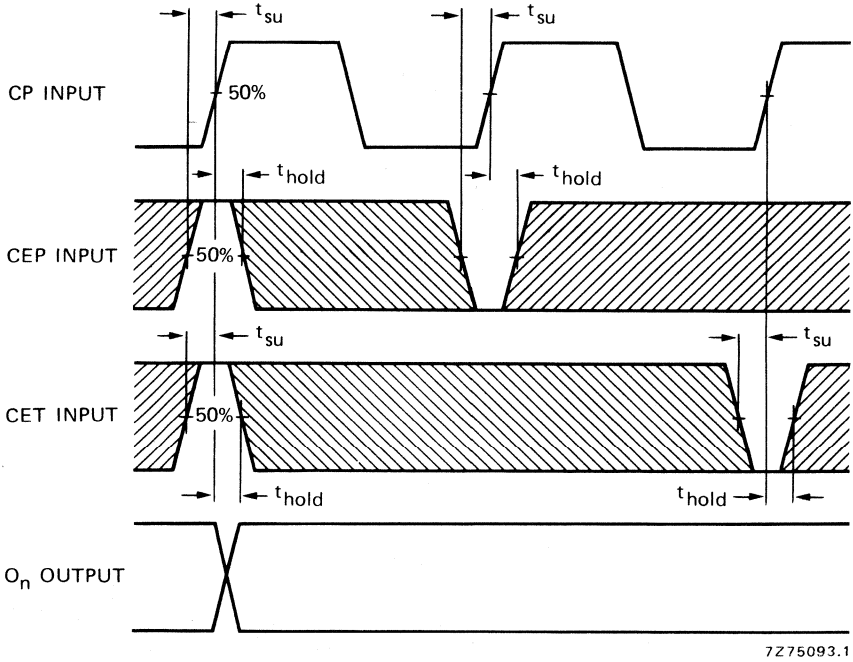
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms on pages 6 and 7
	10		40	20		ns	
	15		30	15		ns	
Minimum $\overline{MR}$ pulse width; LOW	5	t_{WMRL}	100	50		ns	
	10		40	20		ns	
	15		30	15		ns	
Recovery time for $\overline{MR}$	5	t_{RMR}	25	0		ns	
	10		15	0		ns	
	15		10	0		ns	
Set-up times $P_n \longrightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \longrightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
Hold times $P_n \longrightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \longrightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		17	35		MHz	



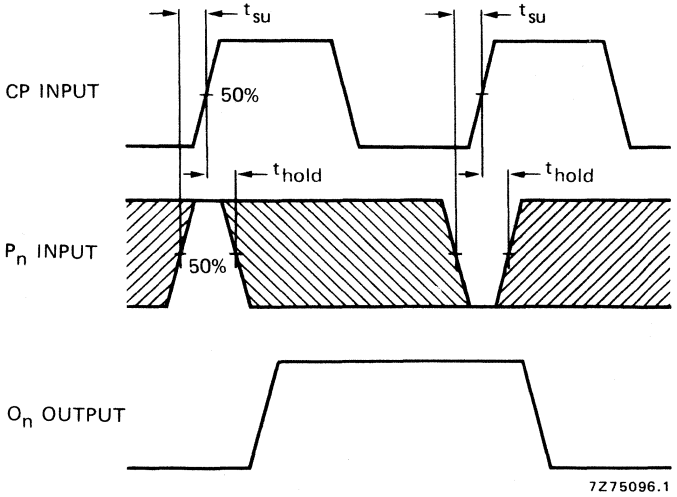
Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Waveforms showing minimum CP and $\overline{MR}$ pulse widths and $\overline{MR}$ to CP recovery time.



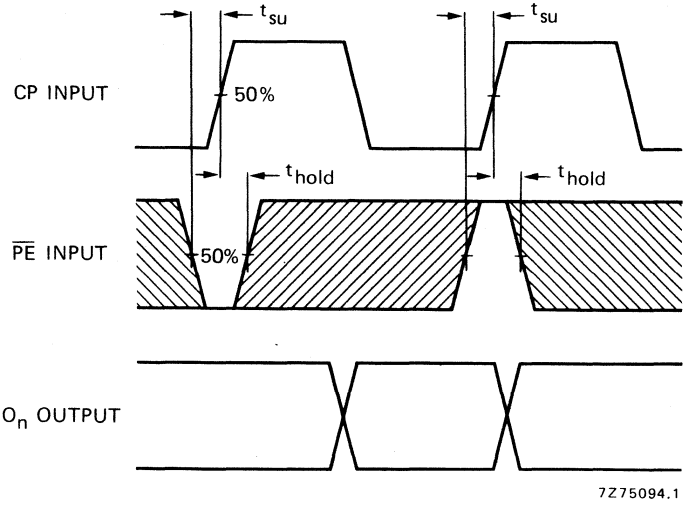
Waveforms showing set-up times and hold times for CEP and CET inputs.

Conditions: $\overline{PE}$ = $\overline{MR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{MR}$ = HIGH

Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{MR}$ = HIGH

Waveforms showing set-up times and hold times for $\overline{PE}$ inputs.

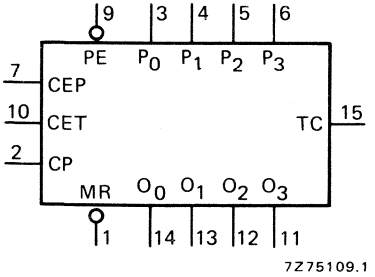
Note

Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT SYNCHRONOUS BINARY COUNTER WITH ASYNCHRONOUS RESET

The HEF40161B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), an overriding asynchronous master reset (MR), four parallel data inputs (P_0 to P_3), three synchronous mode control inputs (parallel enable (PE), count enable parallel (CEP) and count enable trickle (CET)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous (except for the $\overline{MR}$ input) and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise, no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_1 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{MR}$ sets all outputs (O_0 to O_3 and TC) LOW, independent of the state of all other inputs. Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique. CEP, CET and $\overline{PE}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.



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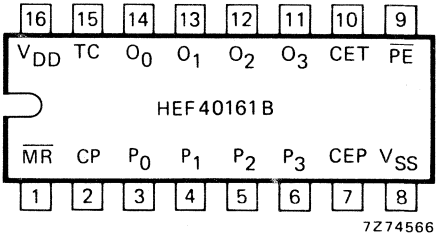

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HEF40161BP: 16-lead DIL; plastic (SOT-38Z).
HEF40161BD: 16-lead DIL; ceramic (SOT-74).

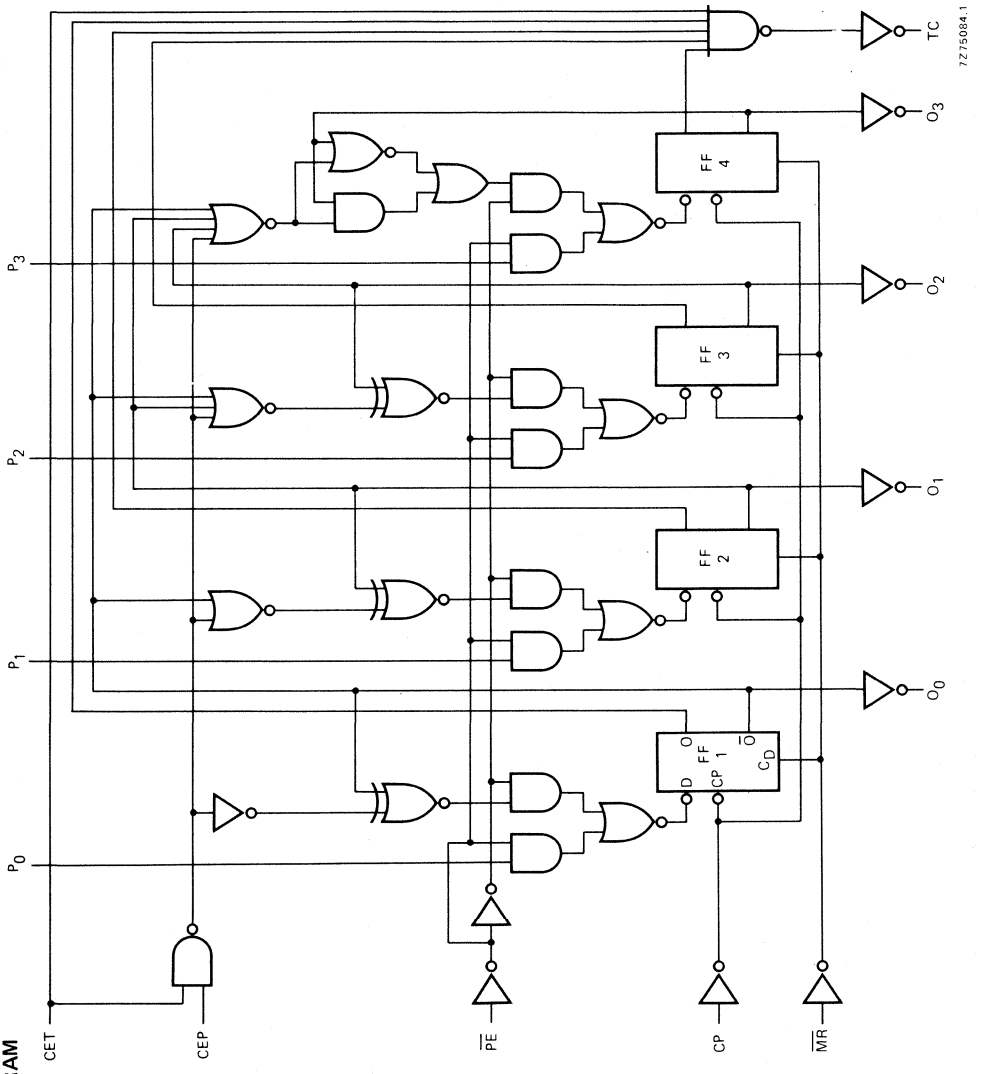
PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOAD DIAGRAM



SYNCHRONOUS MODE SELECTION

$\overline{PE}$	CEP	CET	mode
L	X	X	preset
H	L	X	no change
H	X	L	no change
H	H	H	count

$\overline{MR}$ = HIGH

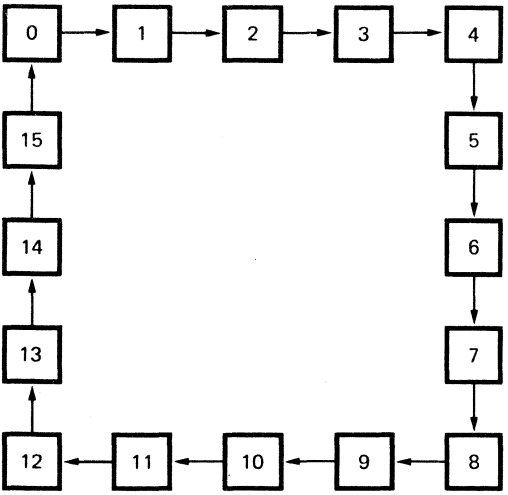
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$

STATE DIAGRAM



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A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	1 200 f_i + Σ($f_o C_L$) × V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) Σ($f_o C_L$) = sum of outputs V_{DD} = supply voltage (V)
	10	5 600 f_i + Σ($f_o C_L$) × V_{DD}^2	
	15	16 000 f_i + Σ($f_o C_L$) × V_{DD}^2	

A.C. CHARACTERISTICS

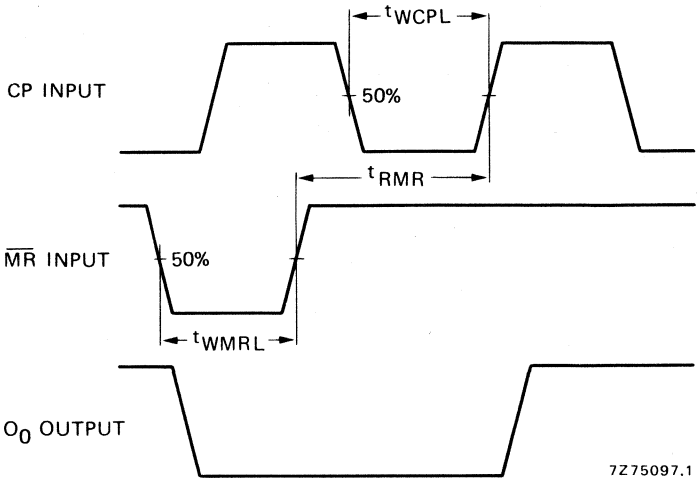
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			120	245	ns	93 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → TC	5			145	295	ns	118 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	85	ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

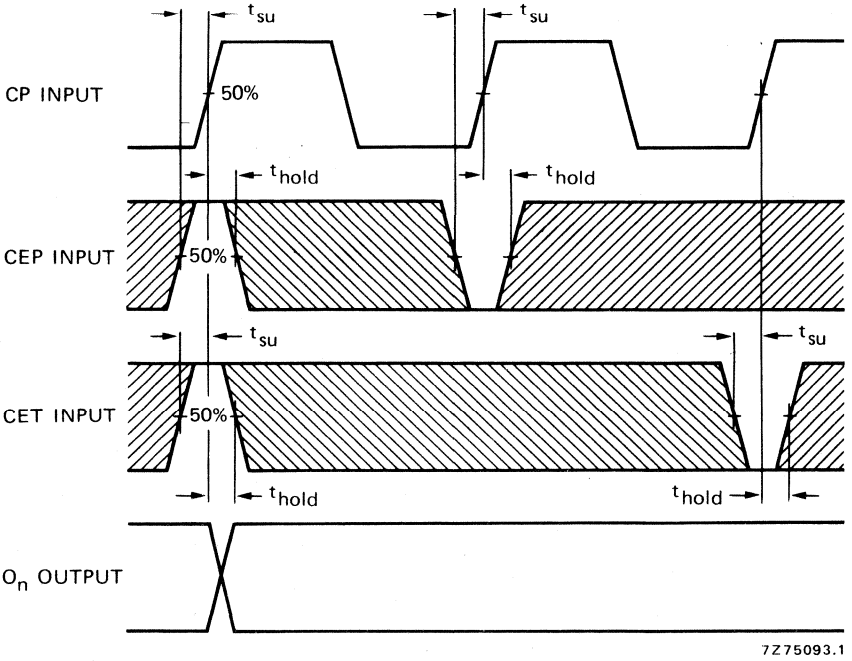
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms on pages 6 and 7
	10		40	20		ns	
	15		30	15		ns	
Minimum $\overline{MR}$ pulse width; LOW	5	t_{WMRL}	100	50		ns	
	10		40	20		ns	
	15		30	15		ns	
Recovery time for $\overline{MR}$	5	t_{RMR}	25	0		ns	
	10		15	0		ns	
	15		10	0		ns	
Set-up times							
$P_n \longrightarrow CP$	5	t_{su}	110	55		ns	
	10		40	20		ns	
	15		30	15		ns	
$\overline{PE} \longrightarrow CP$	5	t_{su}	120	60		ns	
	10		40	20		ns	
	15		25	10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{su}	260	130		ns	
	10		100	50		ns	
	15		70	35		ns	
Hold times							
$P_n \longrightarrow CP$	5	t_{hold}	20	−35		ns	
	10		10	−10		ns	
	15		5	−10		ns	
$\overline{PE} \longrightarrow CP$	5	t_{hold}	15	−45		ns	
	10		5	−15		ns	
	15		5	−10		ns	
CEP, CET $\longrightarrow$ CP	5	t_{hold}	25	−105		ns	
	10		15	−35		ns	
	15		10	−25		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		17	35		MHz	

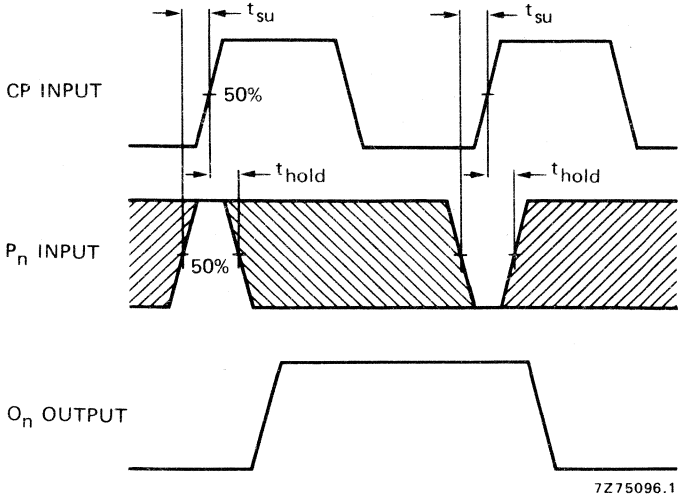


Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Waveforms showing minimum CP and $\overline{MR}$ pulse widths and $\overline{MR}$ to CP recovery time.

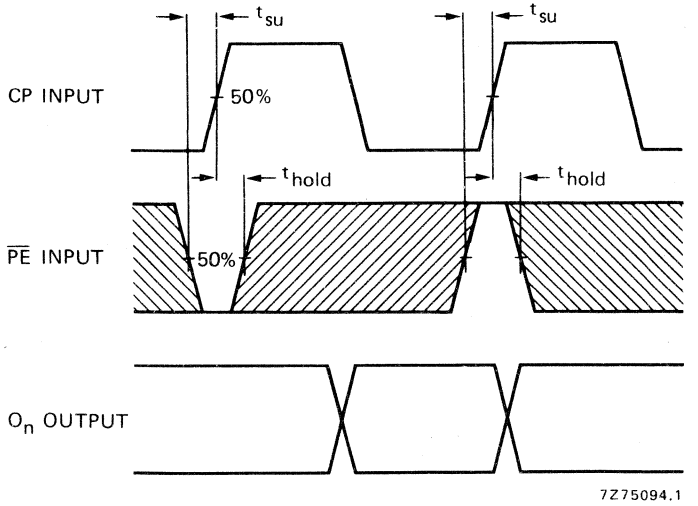


Waveforms showing set-up times and hold times for CEP and CET inputs.
Condition: $\overline{PE}$ = $\overline{MR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{MR}$ = HIGH

Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{MR}$ = HIGH

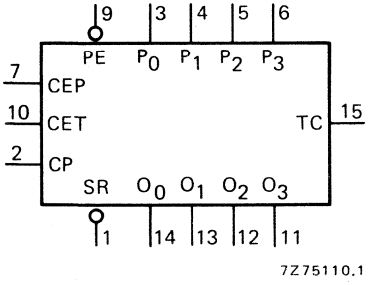
Waveforms showing set-up times and hold times for $\overline{PE}$ input.

Note
Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT SYNCHRONOUS DECADE COUNTER WITH SYNCHRONOUS RESET

The HEF40162B is a fully synchronous edge-triggered 4-bit decade counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 9 ($O_0 = O_3$ = HIGH, $O_1 = O_2$ = LOW) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.



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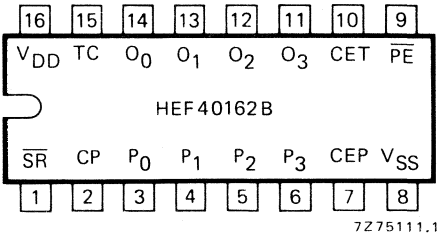

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HEF40162BP: 16-lead DIL; plastic (SOT-38Z).
HEF40162BD: 16-lead DIL; ceramic (SOT-74).

PINNING

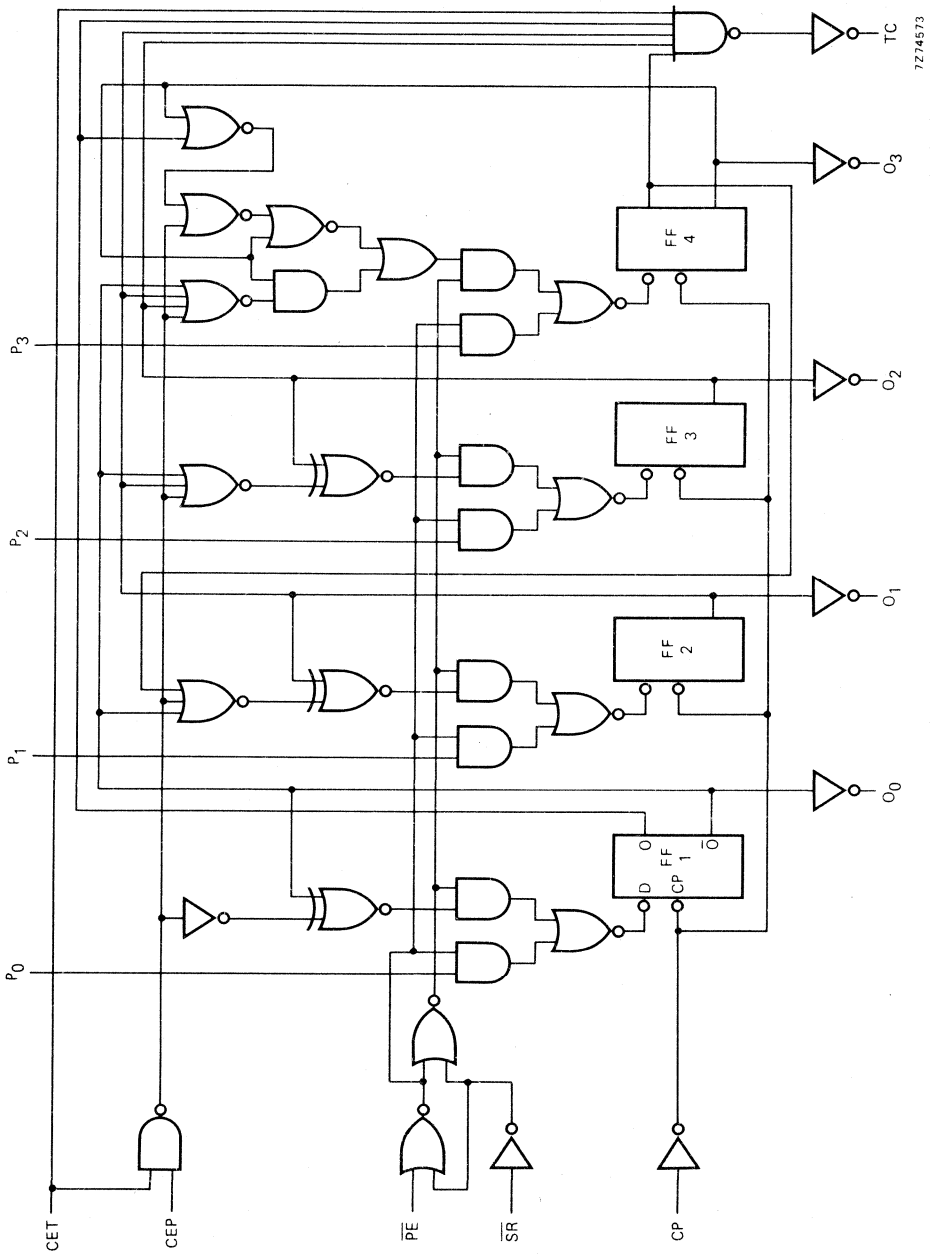
$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{SR}$	synchronous reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

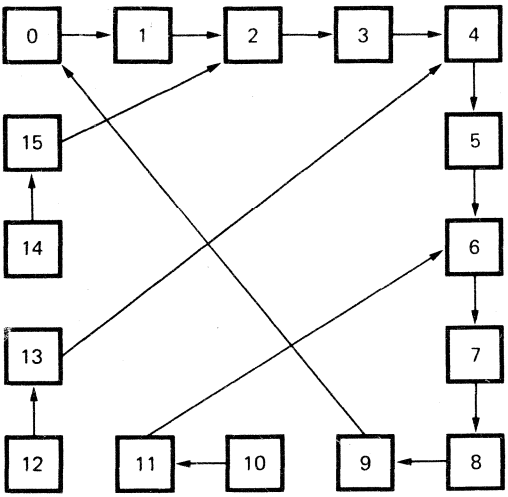
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot O_3$

STATE DIAGRAM



7Z75086

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

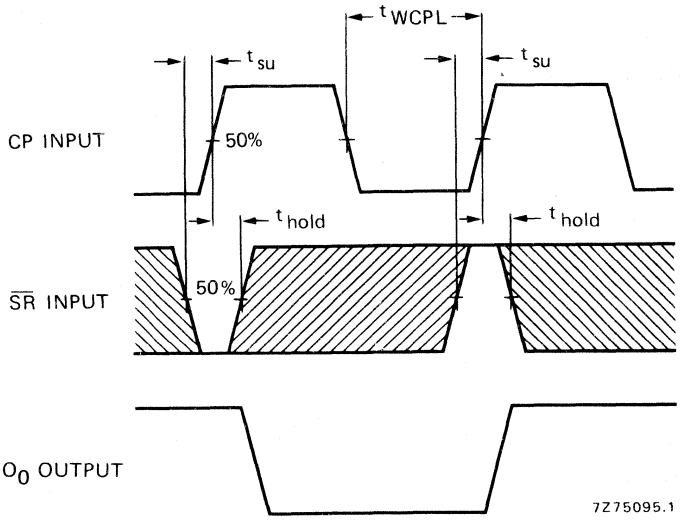
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP → TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET → TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

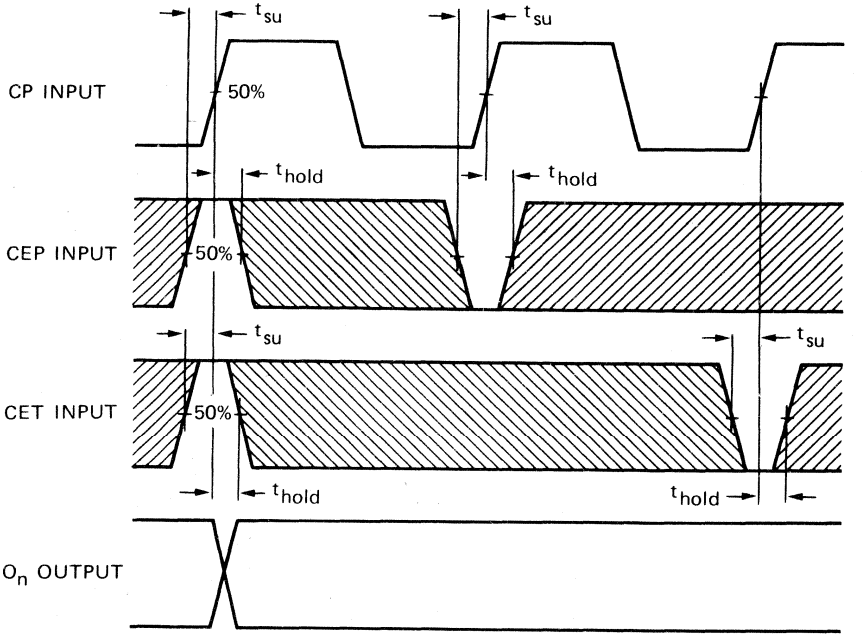
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms on pages 6 and 7
	10		40	20		ns	
	15		30	15		ns	
Set-up times	5		110	55		ns	
$P_n \longrightarrow CP$	10	t_{su}	40	20		ns	
	15		30	15		ns	
	5		120	60		ns	
$\overline{PE} \longrightarrow CP$	10	t_{su}	40	20		ns	
	15		25	10		ns	
	5		260	130		ns	
CEP, CET $\longrightarrow$ CP	10	t_{su}	100	50		ns	
	15		70	35		ns	
	5		50	25		ns	
$\overline{SR} \longrightarrow CP$	10	t_{su}	20	10		ns	
	15		15	10		ns	
Hold times	5		20	−35		ns	
$P_n \longrightarrow CP$	10	t_{hold}	10	−10		ns	
	15		5	−10		ns	
	5		15	−45		ns	
$\overline{PE} \longrightarrow CP$	10	t_{hold}	5	−15		ns	
	15		5	−10		ns	
	5		25	−105		ns	
CEP, CET $\longrightarrow$ CP	10	t_{hold}	15	−35		ns	
	15		10	−25		ns	
	5		15	−10		ns	
$\overline{SR} \longrightarrow CP$	10	t_{hold}	5	−5		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		17	35		MHz	



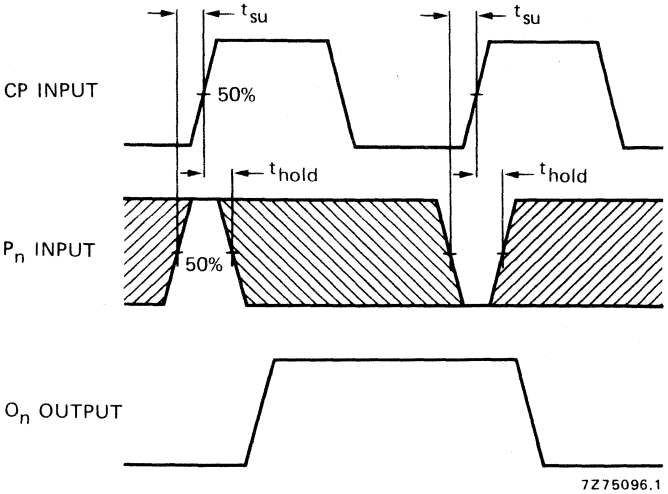
Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Waveforms showing set-up times and hold times for $\overline{SR}$ input and minimum CP pulse width.



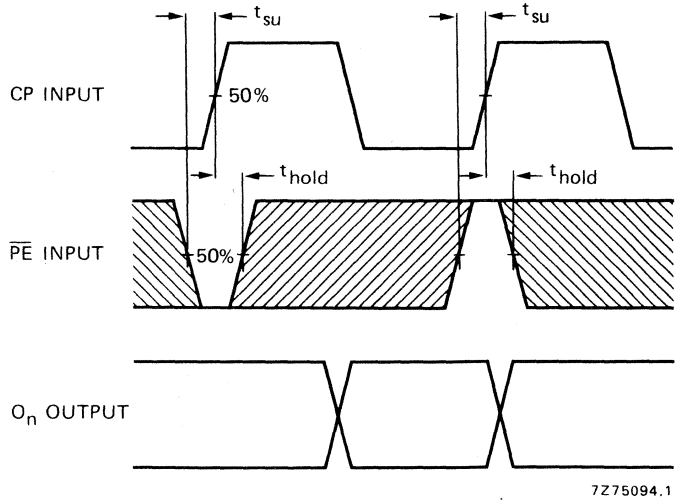
Waveforms showing set-up times and hold times for CEP and CET inputs.

Condition: $\overline{PE}$ = $\overline{SR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{SR}$ = HIGH

Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{SR}$ = HIGH

Waveforms showing set-up times and hold times for $\overline{PE}$ input.

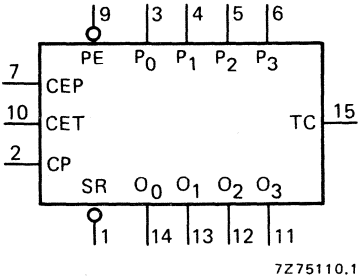
Note

Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT SYNCHRONOUS BINARY COUNTER WITH SYNCHRONOUS RESET

The HEF40163B is a fully synchronous edge-triggered 4-bit binary counter with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), four synchronous mode control inputs (parallel enable ($\overline{PE}$), count enable parallel (CEP), count enable trickle (CET) and synchronous reset ($\overline{SR}$)), buffered outputs from all four bit positions (O_0 to O_3) and a terminal count output (TC).

Operation is fully synchronous and occurs on the LOW to HIGH transition of CP. When $\overline{PE}$ is LOW, the next LOW to HIGH transition of CP loads data into the counter from P_0 to P_3. When $\overline{PE}$ is HIGH, the next LOW to HIGH transition of CP advances the counter to its next state only if both CEP and CET are HIGH; otherwise no change occurs in the state of the counter. TC is HIGH when the state of the counter is 15 (O_0 to O_3 = HIGH) and when CET is HIGH. A LOW on $\overline{SR}$ sets all outputs (O_0 to O_3 and TC) LOW on the next LOW to HIGH transition of CP, independent of the state of all other synchronous mode control inputs (CEP, CET and $\overline{PE}$). Multistage synchronous counting is possible without additional components by using a carry look-ahead counting technique. CEP, CET, $\overline{PE}$ and $\overline{SR}$ must be stable only during the set-up time before the LOW to HIGH transition of CP.



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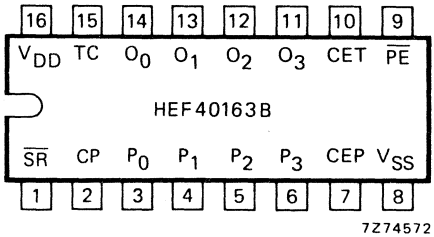


7Z74572

HEF40163BP: 16-lead DIL; plastic (SOT-38Z).
HEF40163BD: 16-lead DIL; ceramic (SOT-74).

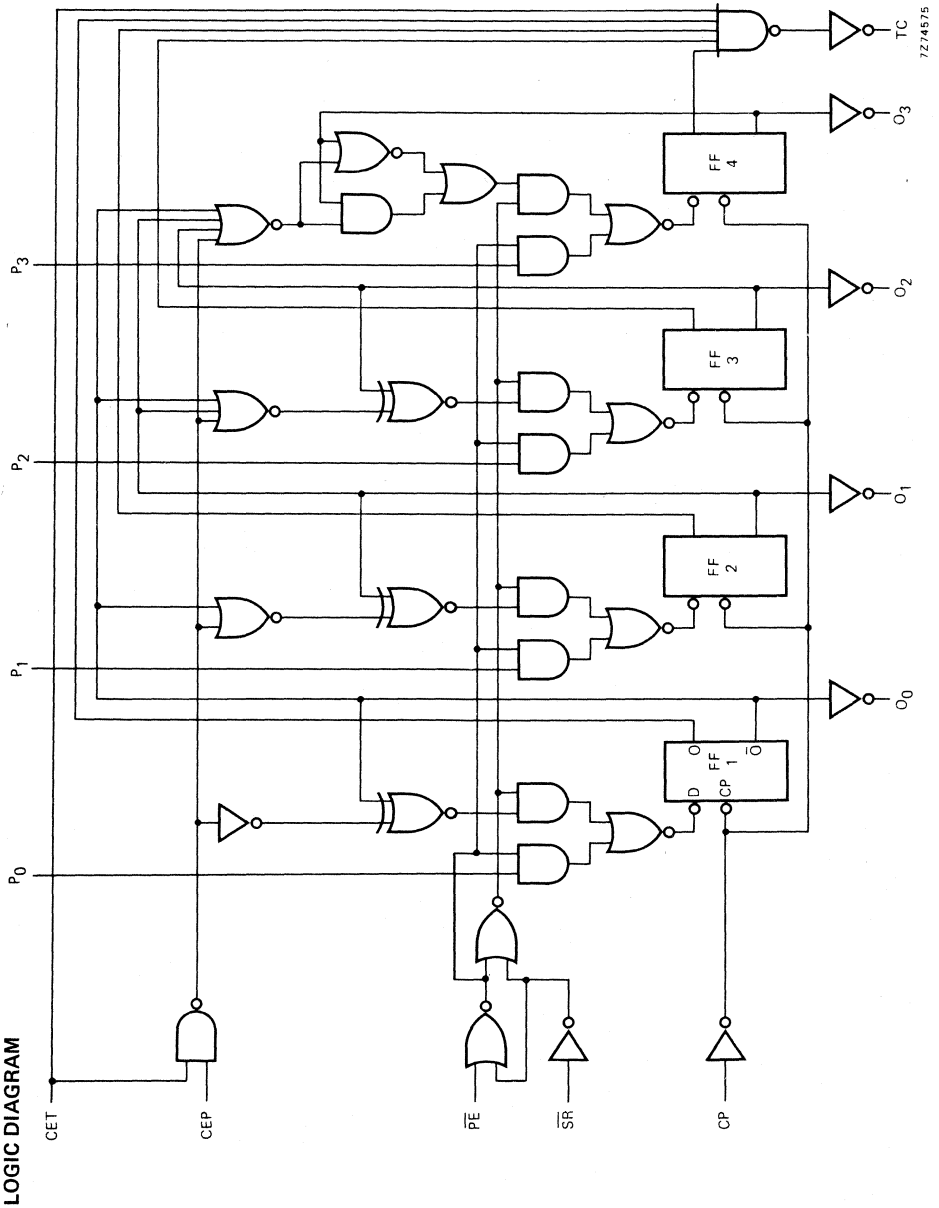
PINNING

$\overline{PE}$	parallel enable input
P_0 to P_3	parallel data inputs
CEP	count enable parallel input
CET	count enable trickle input
CP	clock input (LOW to HIGH, edge-triggered)
$\overline{SR}$	synchronous reset input (active LOW)
O_0 to O_3	parallel outputs
TC	terminal count output

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM



SYNCHRONOUS MODE SELECTION

$\overline{SR}$	$\overline{PE}$	CEP	CET	mode
H	L	X	X	preset
H	H	L	X	no change
H	H	X	L	no change
H	H	H	H	count
L	X	X	X	reset

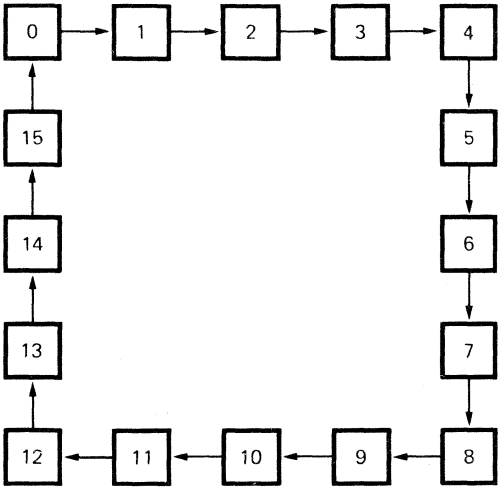
H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

TERMINAL COUNT GENERATION

CET	$(O_0 \cdot O_1 \cdot O_2 \cdot O_3)$	TC
L	L	L
L	H	L
H	L	L
H	H	H

$TC = CET \cdot O_0 \cdot O_1 \cdot O_2 \cdot O_3$

STATE DIAGRAM



7Z75087

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ⩽ 20 ns

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1\,200\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$5\,600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$16\,000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

A.C. CHARACTERISTICS

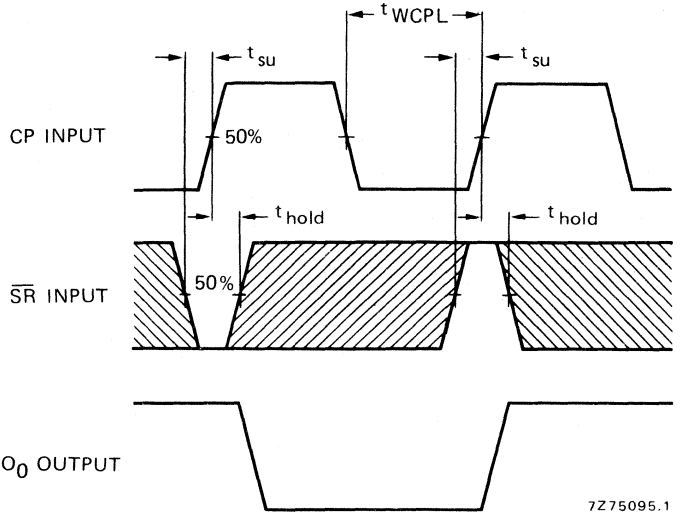
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP ⟶ O_n	5			110	220	ns	83 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			115	230	ns	88 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	95	ns	34 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
CP ⟶ TC	5			130	260	ns	103 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	105	ns	44 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
CET ⟶ TC	5			105	210	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
	5			90	185	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

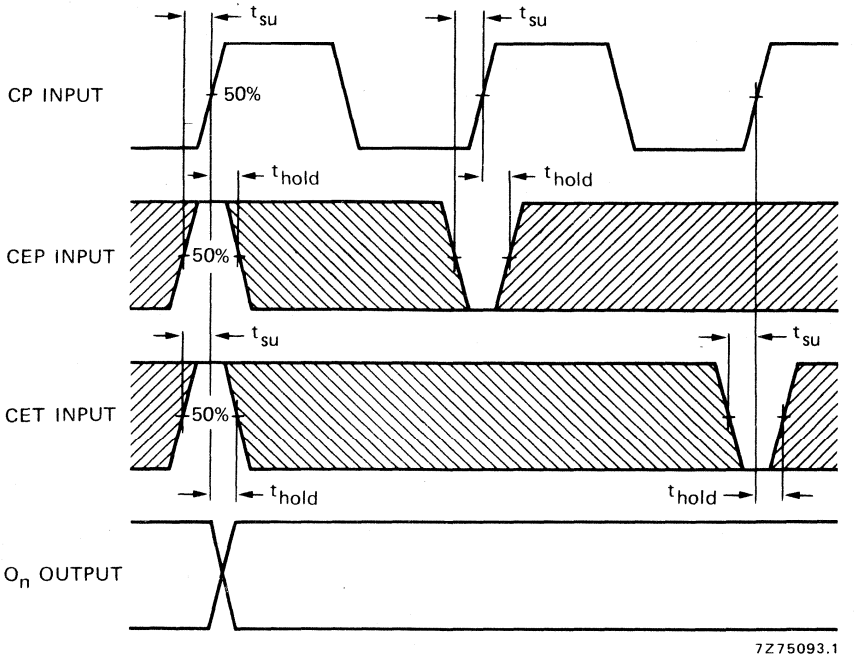
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Minimum clock pulse width; LOW	5	t_{WCPL}	100	50		ns	see also waveforms on pages 6 and 7
	10		40	20		ns	
	15		30	15		ns	
Set-up times	5		110	55		ns	
P_n → CP	10	t_{su}	40	20		ns	
	15		30	15		ns	
	5		120	60		ns	
$\overline{PE}$ → CP	10	t_{su}	40	20		ns	
	15		25	10		ns	
	5		260	130		ns	
CEP, CET → CP	10	t_{su}	100	50		ns	
	15		70	35		ns	
	5		50	25		ns	
$\overline{SR}$ → CP	10	t_{su}	20	10		ns	
	15		15	10		ns	
Hold times	5		20	−35		ns	
P_n → CP	10	t_{hold}	10	−10		ns	
	15		5	−10		ns	
	5		15	−45		ns	
$\overline{PE}$ → CP	10	t_{hold}	5	−15		ns	
	15		5	−10		ns	
	5		25	−105		ns	
CEP, CET → CP	10	t_{hold}	15	−35		ns	
	15		10	−25		ns	
	5		15	−10		ns	
$\overline{SR}$ → CP	10	t_{hold}	5	−5		ns	
	15		5	0		ns	
Maximum clock pulse frequency	5	f_{max}	5	10		MHz	
	10		12	25		MHz	
	15		17	35		MHz	

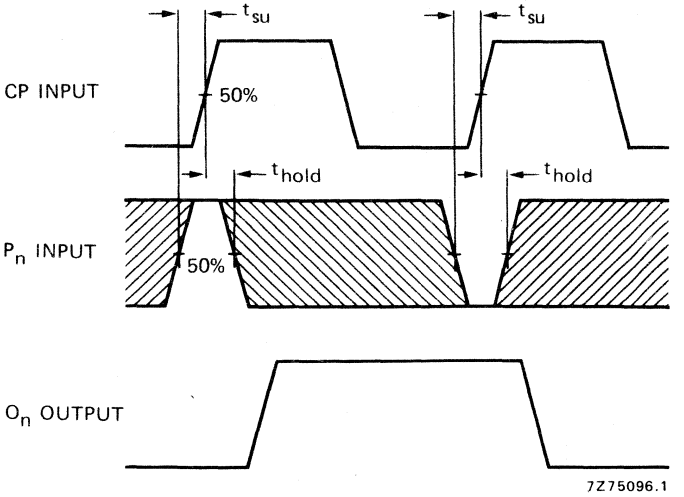


Conditions
$\overline{PE}$ = LOW
P_0 to P_3 = HIGH

Waveforms showing set-up and hold times for $\overline{SR}$ input and minimum CP pulse width.

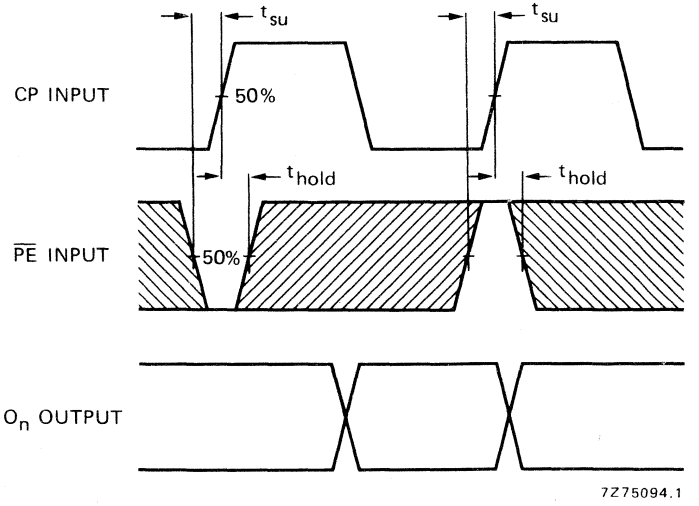


Waveforms showing set-up times and hold times for CEP and CET inputs.
Condition: $\overline{PE}$ = $\overline{SR}$ = HIGH.



Conditions
$\overline{PE}$ = LOW
$\overline{SR}$ = HIGH

Waveforms showing set-up times and hold times for P_n inputs.



Condition
$\overline{SR}$ = HIGH

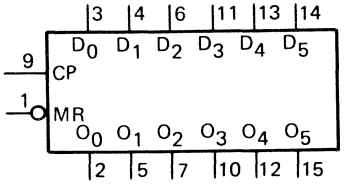
Waveforms showing set-up times and hold times for $\overline{PE}$ input.

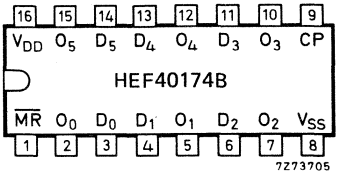
Note

Set-up and hold times are shown as positive values but may be specified as negative values.

HEX D-TYPE FLIP-FLOP

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (O_0 to O_5). Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5.





HEF40174BP: 16-lead DIL; plastic (SOT-38Z).
HEF40174BD: 16-lead DIL; ceramic (SOT-74).

PINNING

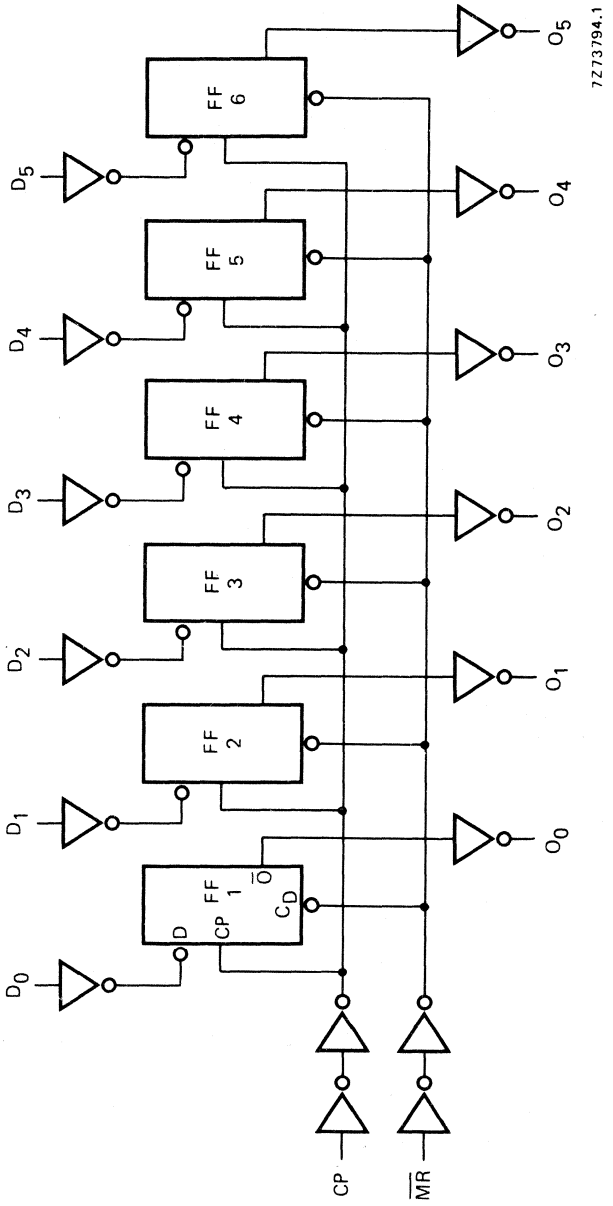
D_0 to D_5	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_5	buffered outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM

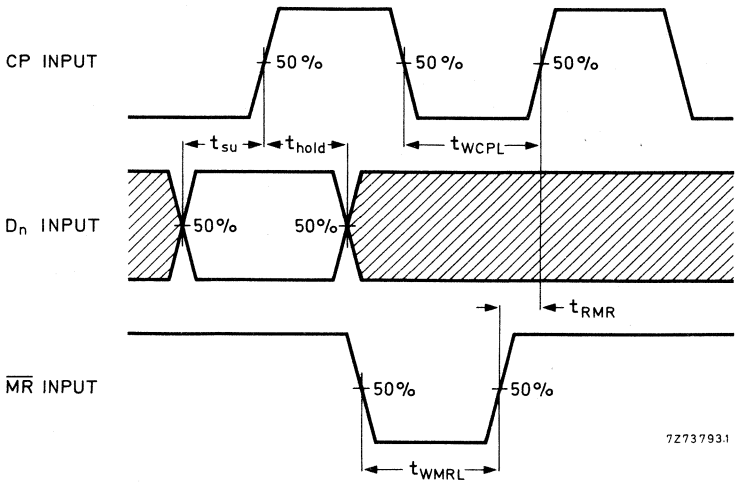


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
	5			75	155	ns	48 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65	ns	19 ns + (0,23 ns/pF) C_L
	15			20	45	ns	12 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	50	ns	17 ns + (0,16 ns/pF) C_L
Set-up time	5		20	10		ns	
D_n → CP	10	t_{su}	10	5		ns	
	15		10	5		ns	
Hold time	5		10	0		ns	
D_n → CP	10	t_{hold}	5	0		ns	
	15		5	0		ns	
Minimum clock	5		70	35		ns	
pulse width; LOW	10	t_{WCPL}	30	15		ns	
	15		20	10		ns	see also waveforms on page 4
Minimum $\overline{MR}$ pulse	5		70	35		ns	
width; LOW	10	t_{WMRL}	35	15		ns	
	15		25	10		ns	
Recovery time	5		45	25		ns	
for $\overline{MR}$	10	t_{RMR}	20	10		ns	
	15		15	5		ns	
Maximum clock	5		5	11		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		20	45		MHz	

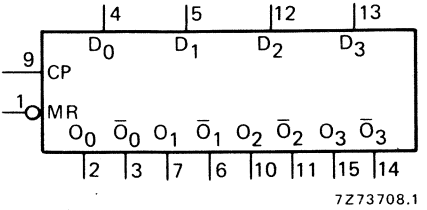
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	3500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	16 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	42 000 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

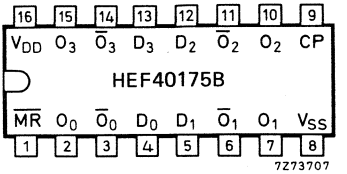


Waveforms showing minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

QUADRUPLE D-TYPE FLIP-FLOP

The HEF40175B is a quadruple edge-triggered D-type flip-flop with four data inputs (D_0 to D_3), a clock input (CP), an overriding asynchronous master reset input ($\overline{MR}$), four buffered outputs (O_0 to O_3), and four complementary buffered outputs ($\overline{O}_0$ to $\overline{O}_3$). Information on D_0 to D_3 is transferred to O_0 to O_3 on the LOW to HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_3 = LOW, $\overline{O}_0$ to $\overline{O}_3$ = HIGH), independent of CP and D_0 to D_3.





HEF40175BP: 16-lead DIL; plastic (SOT-38Z).
HEF40175BD: 16-lead DIL; ceramic (SOT-74).

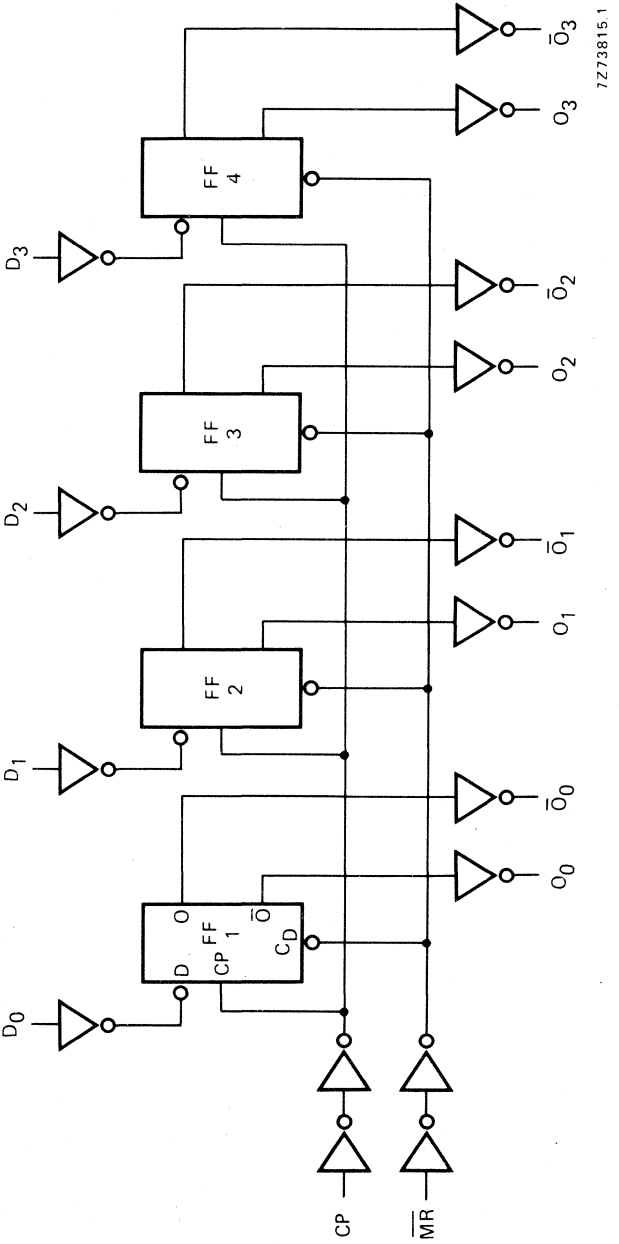
PINNING

D_0 to D_3	data inputs
CP	clock input (LOW to HIGH; edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered outputs
$\overline{O}_0$ to $\overline{O}_3$	complementary buffered outputs

FAMILY DATA

I_{DD} LIMITS category MSI } see Family Specifications

LOGIC DIAGRAM

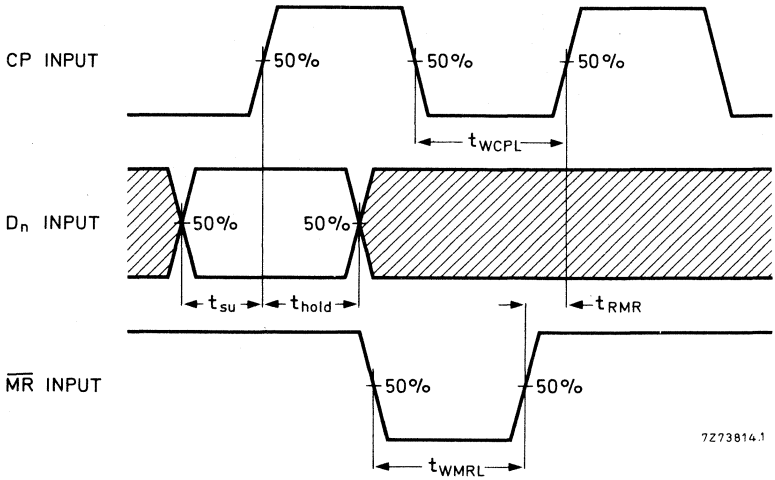


A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
CP ⟶ O_n, $\overline{O}_n$	5			80	160 ns	53 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		35	70 ns	24 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
	5			70	140 ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65 ns	19 ns + (0,23 ns/pF) C_L
	15			25	45 ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ ⟶ O_n	5			75	155 ns	48 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		30	65 ns	19 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ ⟶ $\overline{O}_n$	5			70	140 ns	43 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		30	65 ns	19 ns + (0,23 ns/pF) C_L
	15			25	50 ns	17 ns + (0,16 ns/pF) C_L
Set-up time	5		60	30	ns	
D_n ⟶ CP	10	t_{su}	20	10	ns	
	15		15	5	ns	
Hold time	5		25	−5	ns	
D_n ⟶ CP	10	t_{hold}	10	0	ns	
	15		10	0	ns	
Minimum clock	5		90	45	ns	
pulse width; LOW	10	t_{WCPL}	35	15	ns	
	15		25	10	ns	see also waveforms on page 4
Minimum $\overline{MR}$ pulse	5		80	40	ns	
width; LOW	10	t_{WMRL}	30	15	ns	
	15		20	10	ns	
Recovery time	5		0	−30	ns	
for $\overline{MR}$	10	t_{RMR}	0	−20	ns	
	15		0	−15	ns	
Maximum clock	5		5	11	MHz	
pulse frequency	10	f_{max}	15	30	MHz	
	15		20	45	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$2000\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$8400\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22\,500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

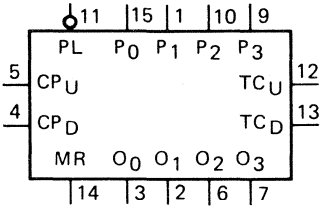


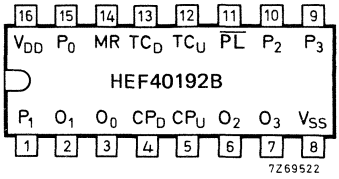
Waveforms showing minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT UP/DOWN DECADE COUNTER

The HEF40192B is a 4-bit synchronous up/down decade counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), a terminal count-up (carry) output (TC_U) and a terminal count-down (borrow) output (TC_D).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. When $\overline{PL}$ is LOW, the information on P_0 to P_3 is loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions.





HEF40192BP : 16-lead DIL; plastic (SOT-38Z).
HEF40192BD: 16-lead DIL; ceramic (SOT-74).

PINNING

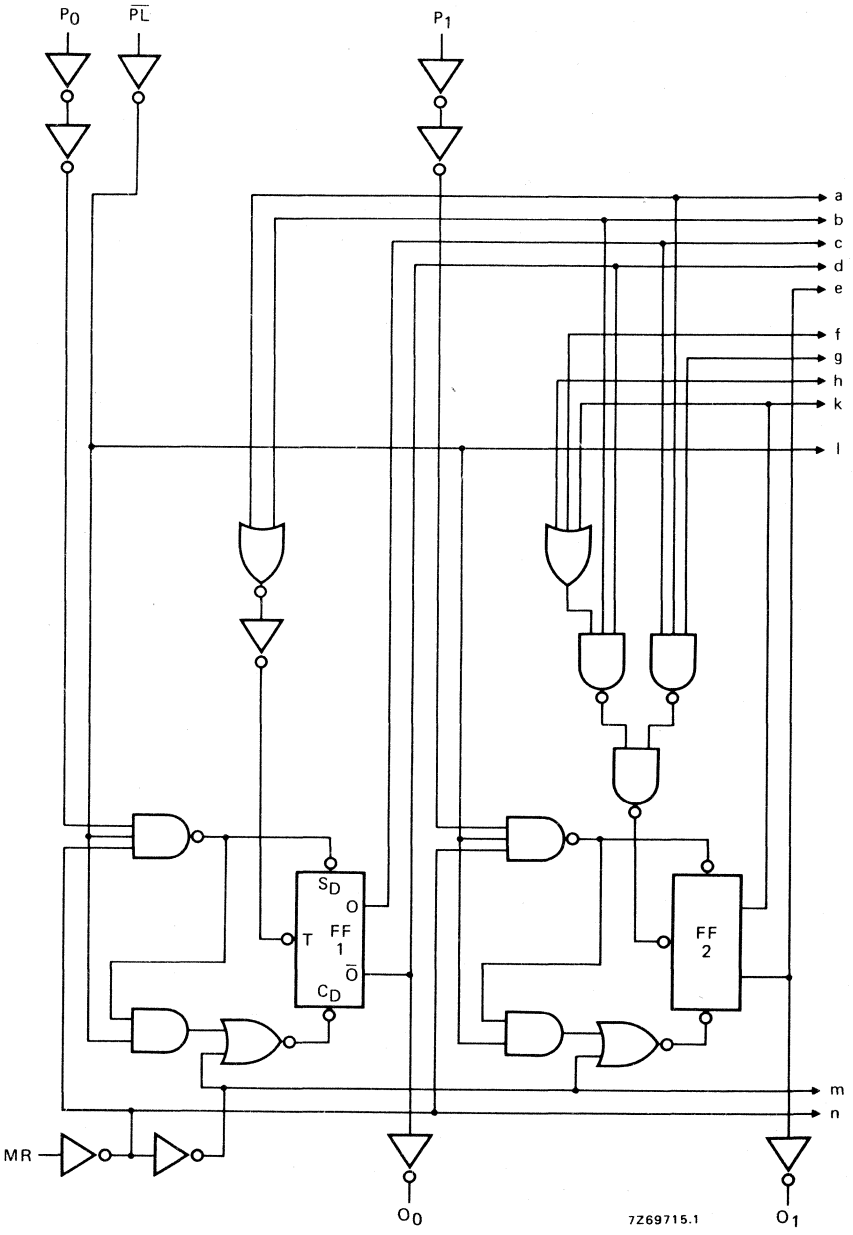
$\overline{PL}$	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
TC_U	buffered terminal count-up (carry) output (active LOW)
TC_D	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA

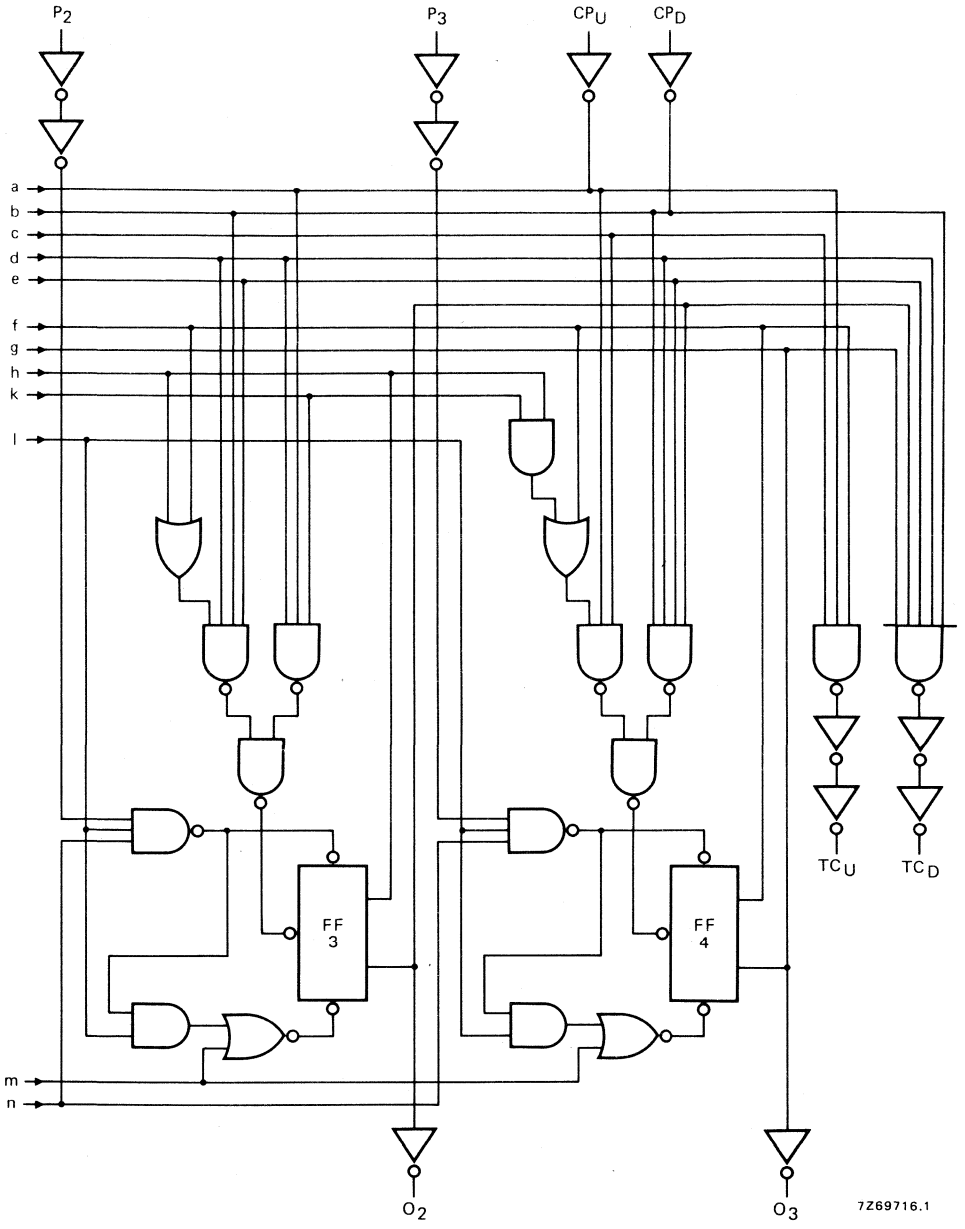
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)

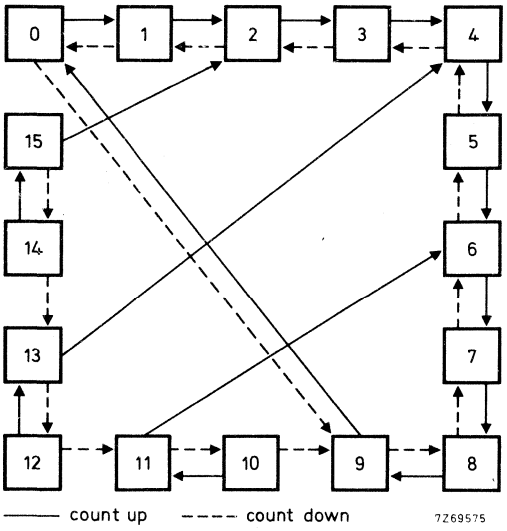


FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	H	H	no change
L	H	∫	H	count-up
L	H	H	∫	count-down

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
∫ = positive-going transition

STATE DIAGRAM



Logic equations for terminal count:

$$TC_U = \overline{O_0 \cdot O_3 \cdot \overline{CP}_U}$$

$$TC_D = \overline{\overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \cdot \overline{CP}_D}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

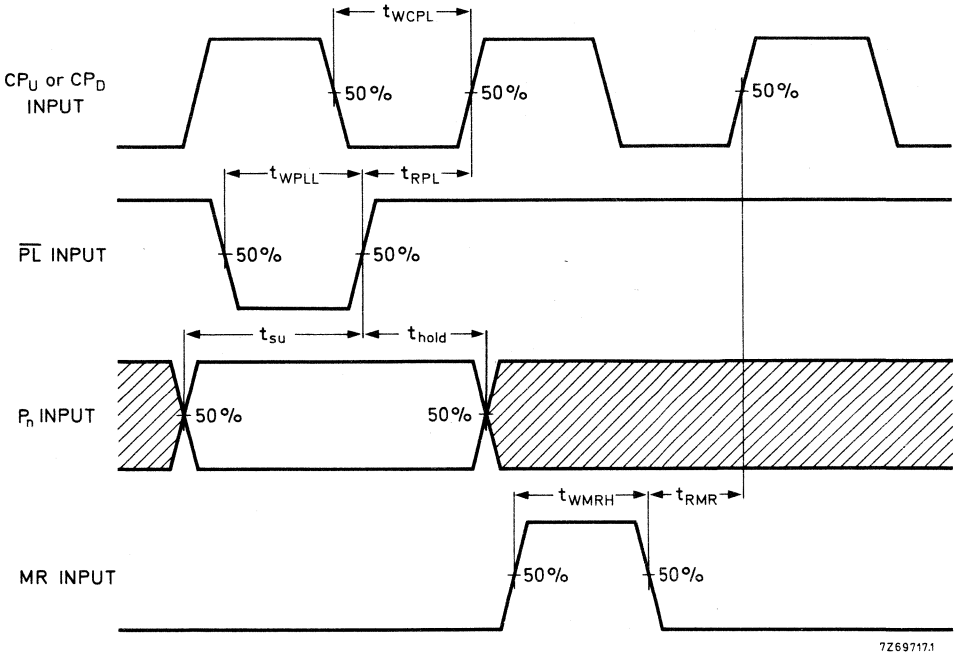
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
$CP_U \rightarrow O_n$	5			210	415	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	165	ns	74 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow O_n$	5			210	420	ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170	ns	74 ns + (0,23 ns/pF) C_L
	15			65	125	ns	57 ns + (0,16 ns/pF) C_L
	5			170	340	ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140	ns	59 ns + (0,23 ns/pF) C_L
	15			50	100	ns	42 ns + (0,16 ns/pF) C_L
$CP_U \rightarrow TC_U$	5			125	250	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			95	185	ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow TC_D$	5			140	280	ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110	ns	44 ns + (0,23 ns/pF) C_L
	15			40	80	ns	32 ns + (0,16 ns/pF) C_L
	5			100	195	ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			195	390	ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160	ns	69 ns + (0,23 ns/pF) C_L
	15			60	120	ns	52 ns + (0,16 ns/pF) C_L
$MR \rightarrow TC_U$	5			145	285	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L
$MR \rightarrow TC_D$	5			365	730	ns	338 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		130	265	ns	119 ns + (0,23 ns/pF) C_L
	15			100	205	ns	92 ns + (0,16 ns/pF) C_L
$\overline{PL} \rightarrow O_n$	5			185	360	ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150	ns	64 ns + (0,23 ns/pF) C_L
	15			55	110	ns	47 ns + (0,16 ns/pF) C_L
	5			145	290	ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120	ns	49 ns + (0,23 ns/pF) C_L
	15			45	90	ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max		
Set-up time $P_n \rightarrow \overline{PL}$	5	t_{su}	160	80		ns	see waveforms on page 7
	10		60	30		ns	
	15		50	25		ns	
Hold time $P_n \rightarrow \overline{PL}$	5	t_{hold}	10	−70		ns	
	10		5	−25		ns	
	15		5	−20		ns	
Minimum CP_U or CP_D pulse width; LOW	5	t_{WCPL}	150	75		ns	
	10		50	25		ns	
	15		35	20		ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	180	90		ns	
	10		70	35		ns	
	15		60	30		ns	
Minimum $\overline{PL}$ pulse width; LOW	5	t_{WPLL}	120	60		ns	
	10		45	20		ns	
	15		30	15		ns	
Recovery time for MR	5	t_{RMR}	125	65		ns	
	10		70	35		ns	
	15		50	25		ns	
Recovery time for $\overline{PL}$	5	t_{RPL}	90	45		ns	
	10		35	15		ns	
	15		25	10		ns	
Maximum clock pulse frequency	5	f_{max}	3	6		MHz	
	10		9	18		MHz	
	15		13	26		MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	550 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	2400 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	
	15	6500 f_i + $\Sigma(f_o C_L)$ x V_{DD}^2	

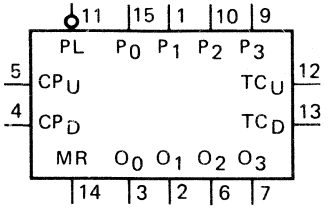


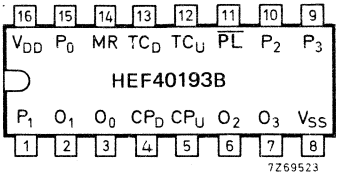
Waveforms showing recovery times for $\overline{PL}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{PL}$ and MR, and set-up and hold times for P to $\overline{PL}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

4-BIT UP/DOWN BINARY COUNTER

The HEF40193B is a 4-bit synchronous up/down binary counter. The counter has a count-up clock input (CP_U), a count-down clock input (CP_D), an asynchronous parallel load input ($\overline{PL}$), four parallel data inputs (P_0 to P_3), an asynchronous master reset input (MR), four counter outputs (O_0 to O_3), a terminal count-up (carry) output (TC_U) and a terminal count-down (borrow) output (TC_D).

The counter outputs change state on the LOW to HIGH transition of either clock input. However, for correct counting, both clock inputs cannot be LOW simultaneously. When $\overline{PL}$ is LOW, the information on P_0 to P_3 is loaded into the counter. A HIGH on MR resets the counter independent of all other input conditions.





HEF40193BP: 16-lead DIL; plastic (SOT-38Z).
HEF40193BD: 16-lead DIL; ceramic (SOT-74).

PINNING

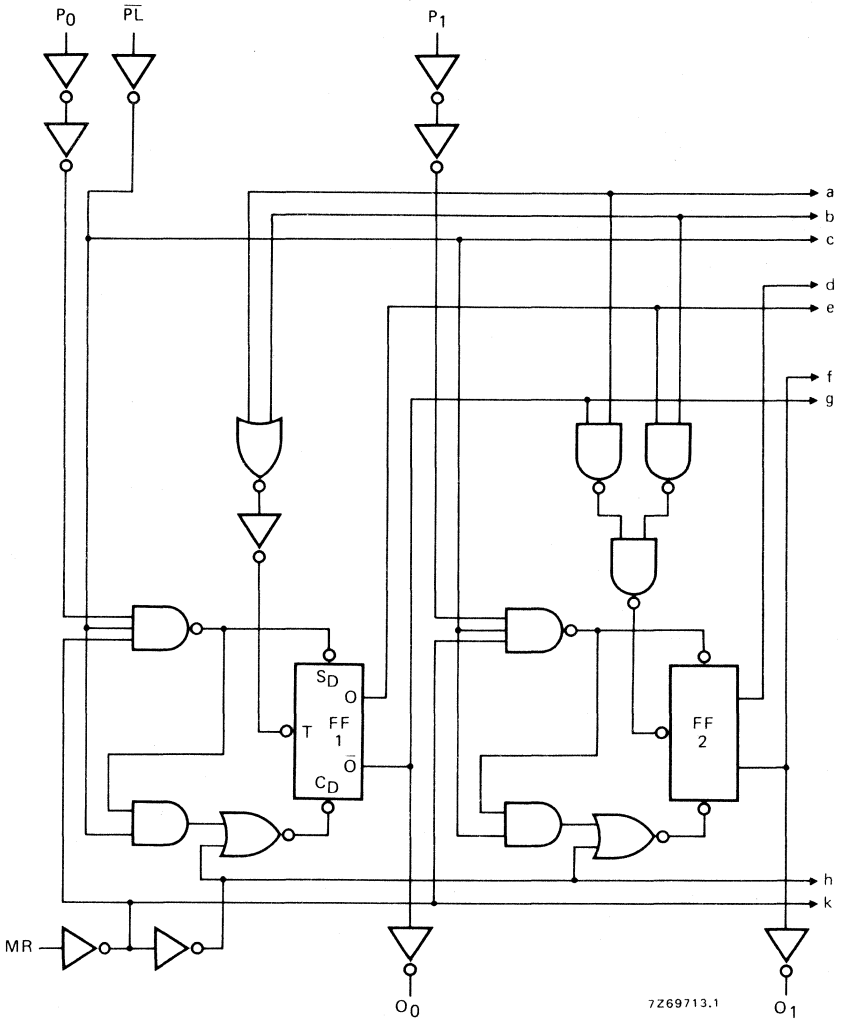
$\overline{PL}$	parallel load input (active LOW)
P_0 to P_3	parallel data inputs
CP_U	count-up clock pulse input (LOW to HIGH, edge-triggered)
CP_D	count-down clock pulse input (LOW to HIGH, edge-triggered)
MR	master reset input (asynchronous)
TC_U	buffered terminal count-up (carry) output (active LOW)
TC_D	buffered terminal count-down (borrow) output (active LOW)
O_0 to O_3	buffered counter outputs

FAMILY DATA

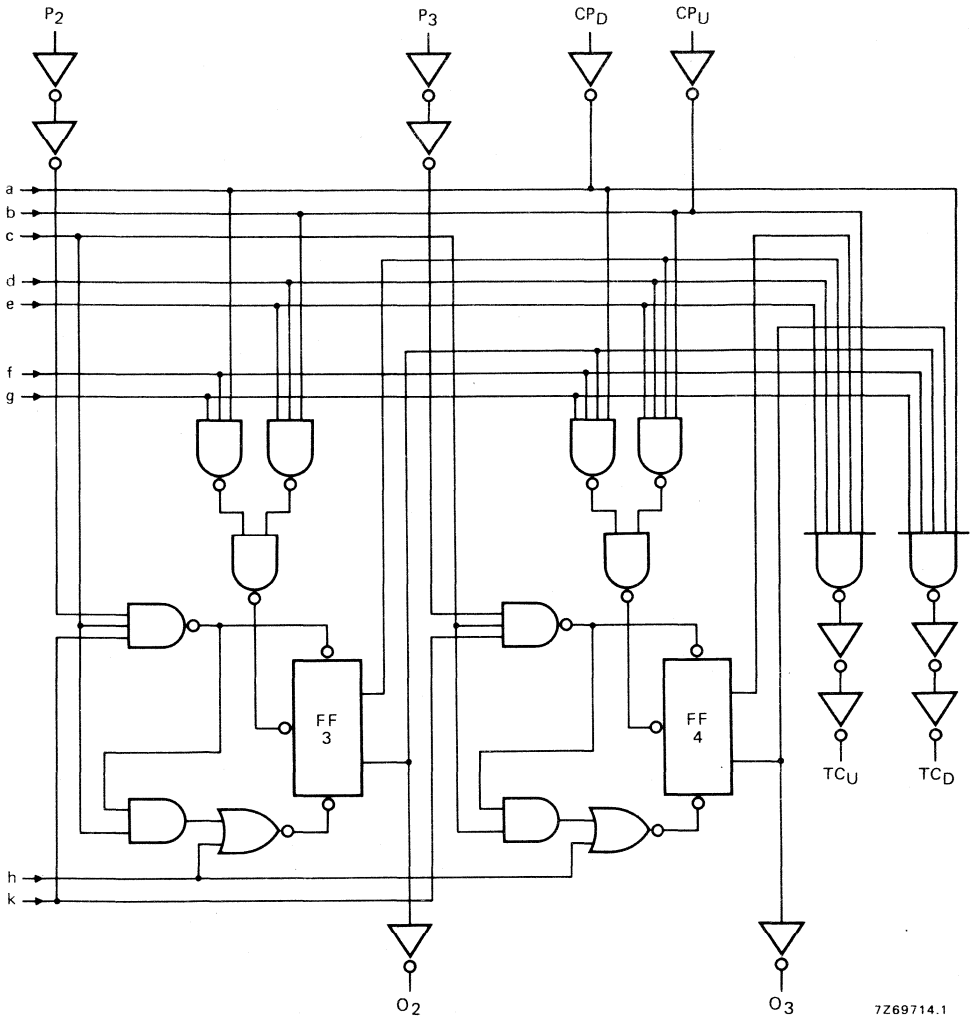
I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



LOGIC DIAGRAM (continued)

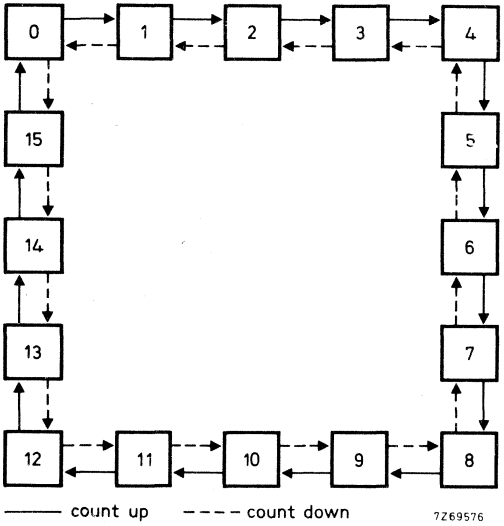


FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	mode
H	X	X	X	reset (asyn.)
L	L	X	X	parallel load
L	H	H	H	no change
L	H	⎍	H	count-up
L	H	H	⎍	count-down

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
⎍ = positive-going transition

STATE DIAGRAM



Logic equations for terminal count:

$$TC_U = \overline{O_0 \cdot O_1 \cdot O_2 \cdot O_3 \cdot \overline{CP}_U}$$

$$TC_D = \overline{\overline{O}_0 \cdot \overline{O}_1 \cdot \overline{O}_2 \cdot \overline{O}_3 \cdot \overline{CP}_D}$$

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

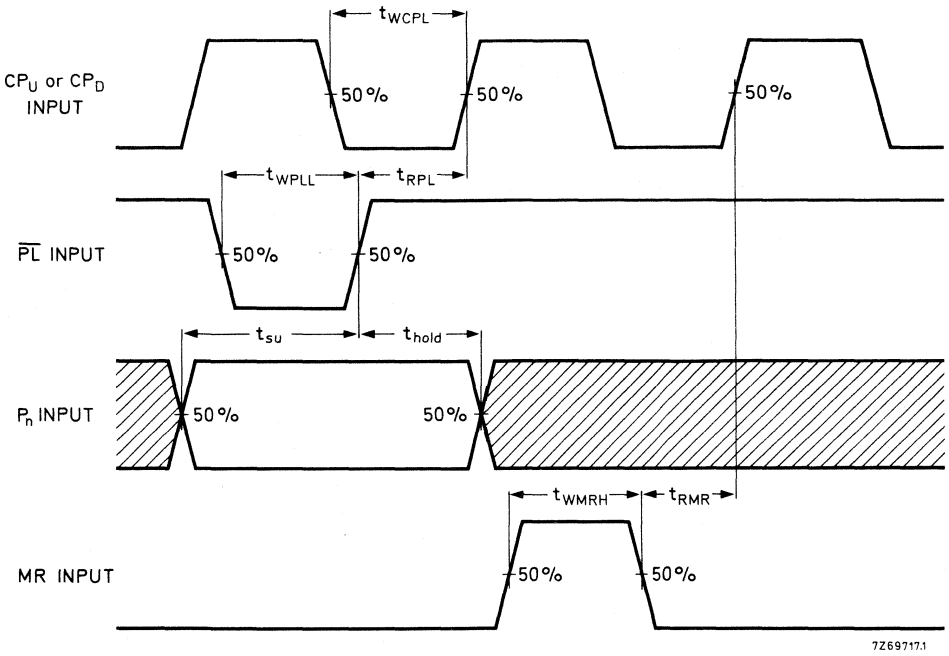
	V_{DD} V	symbol	min	typ	max	typical extrapolation formula
Propagation delays						
$CP_U \rightarrow O_n$	5			210	415 ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	165 ns	74 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow O_n$	5			210	425 ns	183 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		85	170 ns	74 ns + (0,23 ns/pF) C_L
	15			60	125 ns	57 ns + (0,16 ns/pF) C_L
	5			170	340 ns	143 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		70	140 ns	59 ns + (0,23 ns/pF) C_L
	15			50	100 ns	42 ns + (0,16 ns/pF) C_L
$CP_U \rightarrow TC_U$	5			125	250 ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100 ns	39 ns + (0,23 ns/pF) C_L
	15			35	70 ns	27 ns + (0,16 ns/pF) C_L
	5			95	185 ns	68 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80 ns	29 ns + (0,23 ns/pF) C_L
	15			30	60 ns	22 ns + (0,16 ns/pF) C_L
$CP_D \rightarrow TC_D$	5			140	280 ns	113 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		55	110 ns	44 ns + (0,23 ns/pF) C_L
	15			40	80 ns	32 ns + (0,16 ns/pF) C_L
	5			100	195 ns	73 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	85 ns	29 ns + (0,23 ns/pF) C_L
	15			30	65 ns	22 ns + (0,16 ns/pF) C_L
$MR \rightarrow O_n$	5			195	390 ns	168 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		80	160 ns	69 ns + (0,23 ns/pF) C_L
	15			60	120 ns	52 ns + (0,16 ns/pF) C_L
$MR \rightarrow TC_U$	5			145	285 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	115 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L
$MR \rightarrow TC_D$	5			365	730 ns	338 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		130	265 ns	119 ns + (0,23 ns/pF) C_L
	15			100	205 ns	92 ns + (0,16 ns/pF) C_L
$\overline{PL} \rightarrow O_n$	5			185	360 ns	158 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		75	150 ns	64 ns + (0,23 ns/pF) C_L
	15			55	110 ns	47 ns + (0,16 ns/pF) C_L
	5			145	290 ns	118 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		60	120 ns	49 ns + (0,23 ns/pF) C_L
	15			45	90 ns	37 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Set-up time $P_n \rightarrow \overline{PL}$	5	t_{su}	160	80	ns	see waveforms on page 7
	10		60	30	ns	
	15		50	25	ns	
Hold time $P_n \rightarrow \overline{PL}$	5	t_{hold}	10	−70	ns	
	10		5	−25	ns	
	15		5	−20	ns	
Minimum CP_U or CP_D pulse width; LOW	5	t_{WCPL}	150	75	ns	
	10		50	25	ns	
	15		35	20	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	180	90	ns	
	10		70	35	ns	
	15		60	30	ns	
Minimum $\overline{PL}$ pulse width; LOW	5	t_{WPLL}	120	60	ns	
	10		45	20	ns	
	15		30	15	ns	
Recovery time for MR	5	t_{RMR}	125	65	ns	
	10		70	35	ns	
	15		50	25	ns	
Recovery time for $\overline{PL}$	5	t_{RPL}	90	45	ns	
	10		35	15	ns	
	15		25	10	ns	
Maximum clock pulse frequency	5	f_{max}	3	5	MHz	
	10		9	18	MHz	
	15		13	26	MHz	

	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$600\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$2700\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$7500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

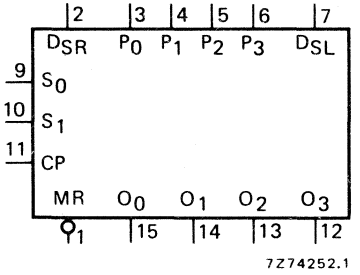


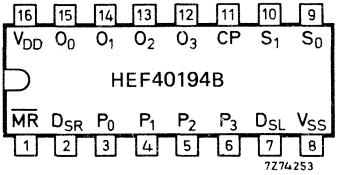
Waveforms showing recovery times for $\overline{PL}$ and MR, minimum pulse widths for CP_U, CP_D, $\overline{PL}$ and MR, and set-up and hold times for P to $\overline{PL}$. Set-up times and hold times are shown as positive values but may be specified as negative values.

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs (S_0 and S_1), a clock input (CP), a serial data shift left input (D_{SL}), a serial data shift right input (D_{SR}), four parallel data inputs (P_0 to P_3), an overriding asynchronous master reset input ($\overline{MR}$), and four buffered parallel outputs (O_0 to O_3). When LOW, $\overline{MR}$ resets all stages and forces O_0 to O_3 LOW, overriding all other input conditions. When $\overline{MR}$ is HIGH, the operation mode is controlled by S_0 and S_1 as shown in the truth table on page 3.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and S_0, S_1 must be stable for a set-up time before the LOW to HIGH transition of CP.





HEF40194BP: 16-lead DIL; plastic (SOT-38Z).
HEF40194BD: 16-lead DIL; ceramic (SOT-74).

PINNING

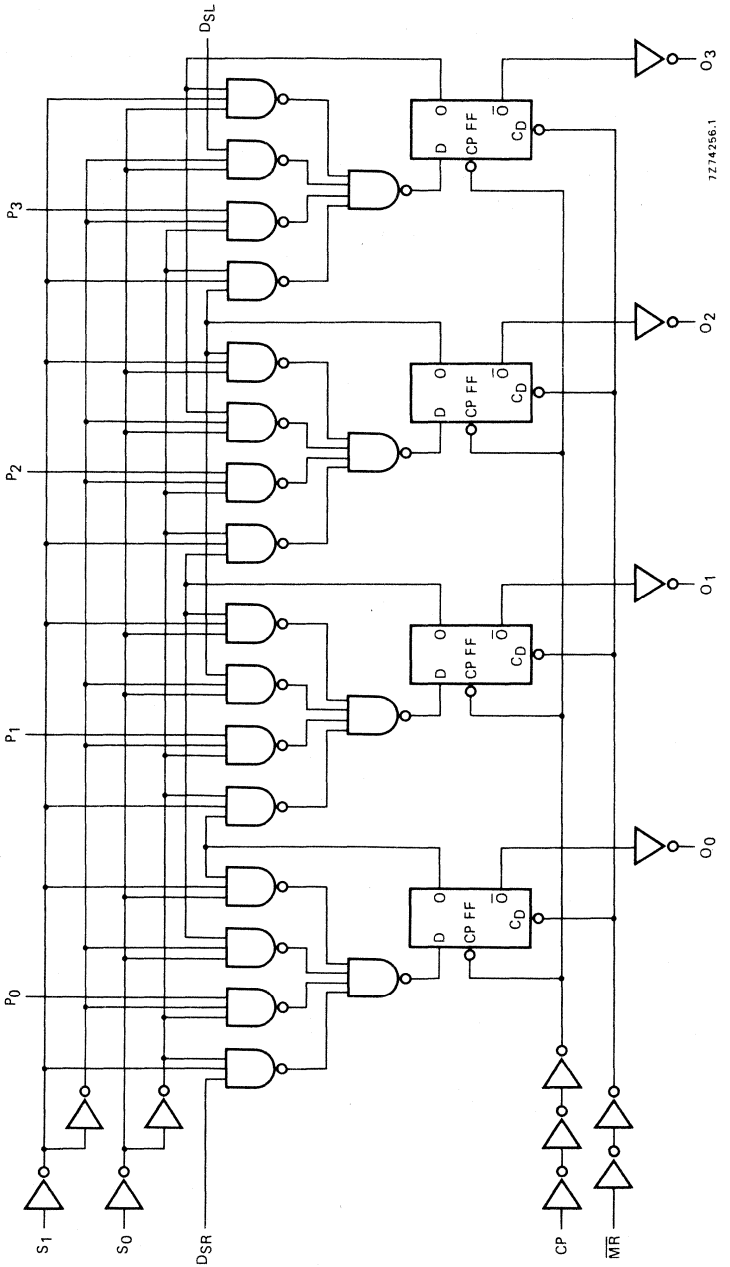
S_0, S_1	mode control inputs
P_0 to P_3	parallel data inputs
D_{SR}	serial data shift right input
D_{SL}	serial data shift left input
CP	clock input (LOW to HIGH edge-triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

operating mode	inputs ($\overline{MR}$ = HIGH)					outputs at t_{n+1}			
	S_1	S_0	D_{SR}	D_{SL}	P_0 to P_3	O_0	O_1	O_2	O_3
hold	L	L	X	X	X	O_0	O_1	O_2	O_3
shift left	H	L	X	L	X	O_1	O_2	O_3	L
	H	L	X	H	X	O_1	O_2	O_3	H
shift right	L	H	L	X	X	L	O_0	O_1	O_2
	L	H	H	X	X	H	O_0	O_1	O_2
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
t_{n+1} = state after next LOW to HIGH transition of CP

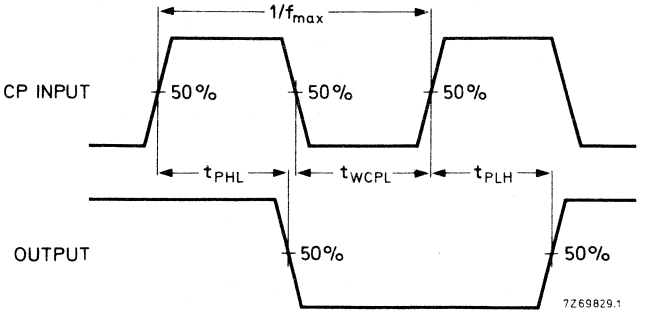
A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

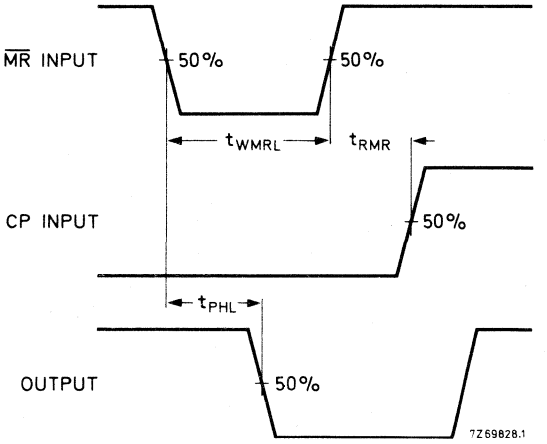
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			100	205	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	85	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
	5			80	165	ns	53 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		35	70	ns	24 ns + (0,23 ns/pF) C_L
	15			25	55	ns	17 ns + (0,16 ns/pF) C_L
$\overline{MR}$ → O_n	5			85	175	ns	58 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	29 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
Set-up times	5		80	40		ns	
P_n,D_{SR},D_{SL} → CP	10	t_{su}	30	15		ns	
	15		20	10		ns	
	5		140	70		ns	
S_n → CP	10	t_{su}	60	30		ns	
	15		40	20		ns	
Hold times	5		10	−30		ns	
P_n,D_{SR},D_{SL} → CP	10	t_{hold}	5	−10		ns	
	15		5	−5		ns	
	5		25	−45		ns	
S_n → CP	10	t_{hold}	15	−15		ns	
	15		10	−10		ns	
Minimum clock	5			50	25	ns	
pulse width; LOW	10	t_{WCPL}		20	10	ns	
	15			20	10	ns	
Minimum $\overline{MR}$ pulse	5			80	40	ns	
width; LOW	10	t_{WMRL}		40	20	ns	
	15			30	15	ns	
Recovery time	5			30	10	ns	
for $\overline{MR}$	10	t_{RMR}		15	5	ns	
	15			15	5	ns	
Maximum clock	5			6	12	MHz	
pulse frequency	10	f_{max}		15	30	MHz	
	15			20	40	MHz	

see also waveforms on pages 5, 6 and 7

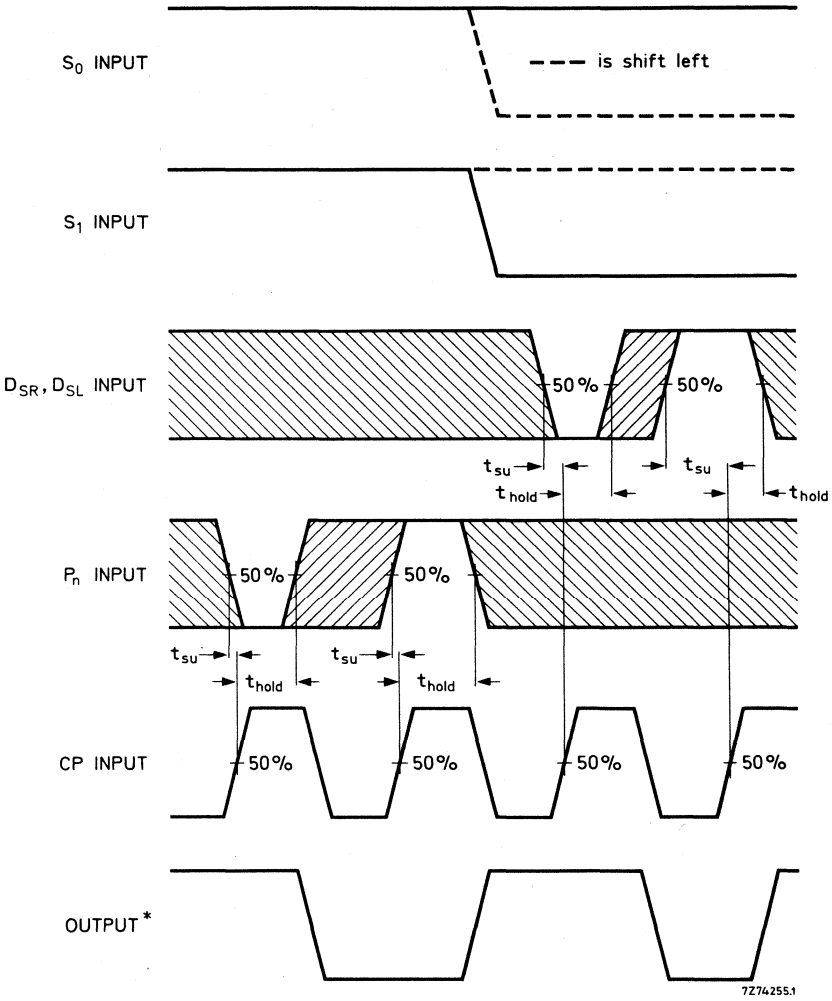
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1500\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$6900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$18\,900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing minimum CP pulse width and CP to output delays
Other conditions: S_1 = LOW; S_0 = HIGH; $\overline{MR}$ = HIGH

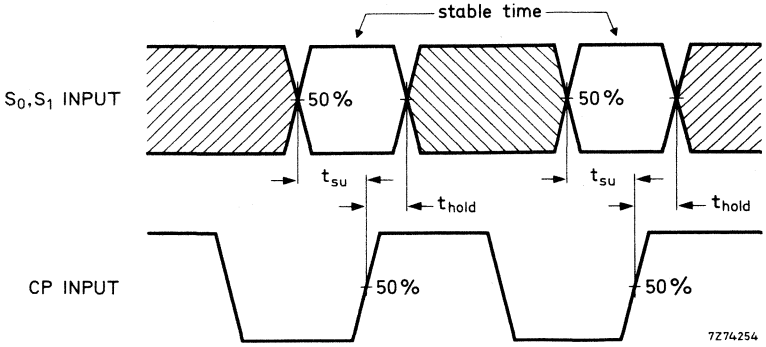


Waveforms showing minimum $\overline{MR}$ pulse width, $\overline{MR}$ to output delays and $\overline{MR}$ to CP recovery time
Other conditions: $S_0 = S_1$ = HIGH; $P_0 = P_1 = P_2 = P_3$ = HIGH



Waveforms showing set-up times, hold times for D_{SR}, D_{SL} and P_n inputs
Other conditions: $\overline{MR}$ = HIGH

* D_{SR} set-up time affects O_0 only; D_{SL} set-up time affects O_3 only.



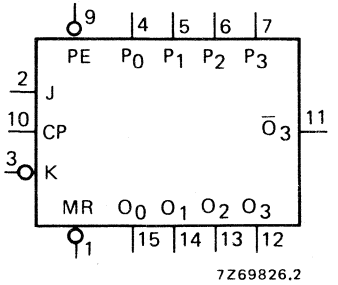
Waveforms showing set-up times and hold times for S_0 and S_1 inputs
Other conditions: $\overline{MR}$ = HIGH

Note

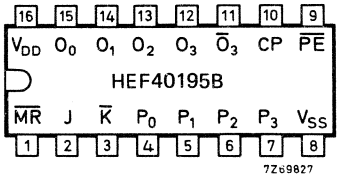
Set-up and hold times are shown as positive values but may be specified as negative values.

4-BIT UNIVERSAL SHIFT REGISTER

The HEF40195B is a fully synchronous edge-triggered 4-bit shift register with a clock input (CP), four synchronous parallel data inputs (P_0 to P_3), two synchronous serial data inputs (J, $\overline{K}$), a synchronous parallel enable input ($\overline{PE}$), buffered parallel outputs from all 4-bit positions (O_0 to O_3), a buffered inverted output from the last bit position ($\overline{O}_3$) and an overriding asynchronous master reset input ($\overline{MR}$). Operation is synchronous (except for $\overline{MR}$) and is edge-triggered on the LOW to HIGH transition of the CP input. When $\overline{PE}$ is LOW, data are loaded into the register from P_0 to P_3 on the LOW to HIGH transition of CP. When $\overline{PE}$ is HIGH, data are shifted into the first register position from J and $\overline{K}$ and all the data in the register are shifted one position to the right on the LOW to HIGH transition of CP.
D-type entry is obtained by interconnecting J and $\overline{K}$.
A LOW on $\overline{MR}$ resets all four bit positions (O_0 to O_3 = LOW, $\overline{O}_3$ = HIGH) independent of all other input conditions.



7Z69826.2



7Z69827

HEF40195BP : 16-lead DIL; plastic (SOT-38Z).
HEF40195BD: 16-lead DIL; ceramic (SOT-74).

PINNING

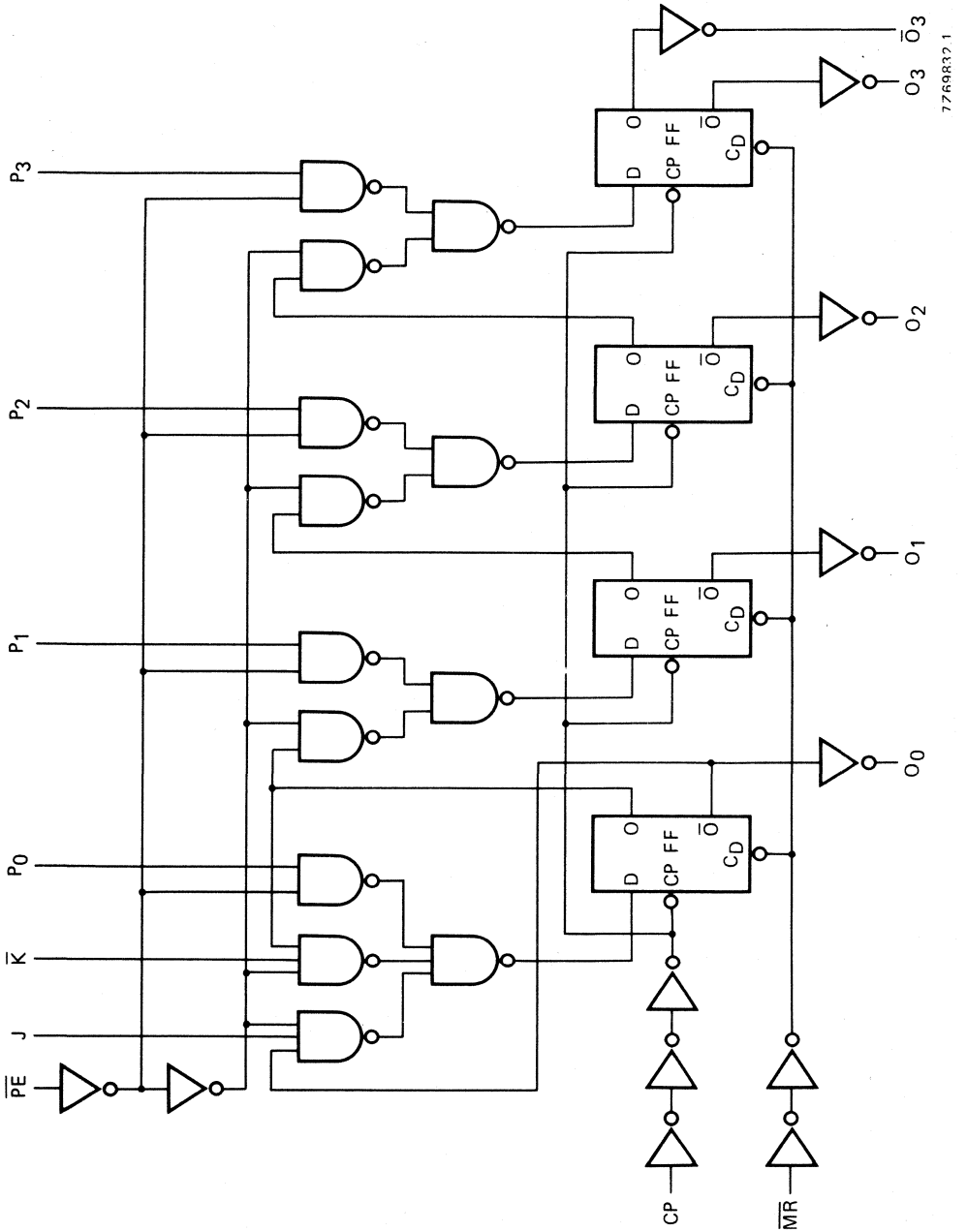
$\overline{PE}$	parallel enable input (active LOW)
P_0 to P_3	parallel data inputs
J	first stage J-input (active HIGH)
$\overline{K}$	first stage K-input (active LOW)
CP	clock input (LOW to HIGH edge triggered)
$\overline{MR}$	master reset input (active LOW)
O_0 to O_3	buffered parallel outputs
$\overline{O}_3$	buffered inverted output from last stage

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

LOGIC DIAGRAM



TRUTH TABLE

operating mode	inputs ($\overline{MR}$ = HIGH)							outputs at $t_n + 1$				
	$\overline{PE}$	J	$\overline{K}$	P_0	P_1	P_2	P_3	O_0	O_1	O_2	O_3	$\overline{O}_3$
shift mode	H	L	L	X	X	X	X	L	O_0	O_1	O_2	$\overline{O}_2$
	H	L	H	X	X	X	X	$\overline{O}_0$	O_0	O_1	O_2	$\overline{O}_2$
	H	H	L	X	X	X	X	$\overline{O}_0$	O_0	O_1	O_2	$\overline{O}_2$
	H	H	H	X	X	X	X	H	O_0	O_1	O_2	$\overline{O}_2$
parallel entry mode	L	X	X	L	L	L	L	L	L	L	L	H
	L	X	X	H	H	H	H	H	H	H	H	L

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
$t_n + 1$ = state after next LOW to HIGH transition of CP

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

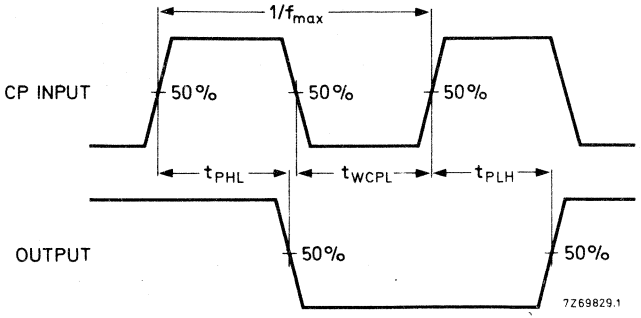
	V_{DD} V	symbol	min	typ	max		typical extrapolation formula
Propagation delays							
CP → O_n	5			105	215	ns	78 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	95	ns	39 ns + (0,23 ns/pF) C_L
	15			35	65	ns	27 ns + (0,16 ns/pF) C_L
	5			90	180	ns	63 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		45	85	ns	34 ns + (0,23 ns/pF) C_L
	15			30	60	ns	22 ns + (0,16 ns/pF) C_L
CP → $\overline{O}_3$	5			125	255	ns	98 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		50	100	ns	39 ns + (0,23 ns/pF) C_L
	15			35	70	ns	27 ns + (0,16 ns/pF) C_L
	5			120	240	ns	93 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		50	105	ns	39 ns + (0,23 ns/pF) C_L
	15			35	75	ns	27 ns + (0,16 ns/pF) C_L
MR → O_n	5			100	205	ns	73 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		45	90	ns	34 ns + (0,23 ns/pF) C_L
	15			30	65	ns	22 ns + (0,16 ns/pF) C_L
	5			125	235	ns	98 ns + (0,55 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		55	115	ns	44 ns + (0,23 ns/pF) C_L
	15			40	85	ns	32 ns + (0,16 ns/pF) C_L

A.C. CHARACTERISTICS

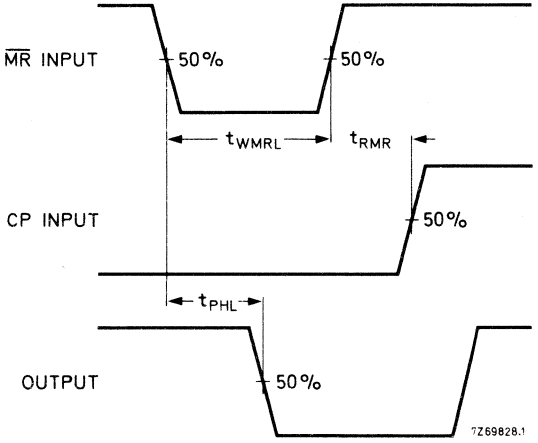
V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	min	typ	max	
Set-up times	5		70	35	ns	see also waveforms on pages 5, 6 and 7
J, $\overline{K}$ → CP	10	t_{su}	20	10	ns	
	15		10	5	ns	
	5		85	40	ns	
P_n → CP	10	t_{su}	25	10	ns	
	15		10	5	ns	
	5		115	55	ns	
$\overline{PE}$ → CP	10	t_{su}	45	20	ns	
	15		30	15	ns	
Hold times	5		15	−20	ns	
J, $\overline{K}$ → CP	10	t_{hold}	5	−5	ns	
	15		0	−5	ns	
	5		20	−25	ns	
P_n → CP	10	t_{hold}	10	−5	ns	
	15		0	−5	ns	
	5		10	−50	ns	
$\overline{PE}$ → CP	10	t_{hold}	5	−20	ns	
	15		5	−10	ns	
Minimum clock	5		60	30	ns	
pulse width; LOW	10	t_{WCPL}	25	10	ns	
	15		20	10	ns	
Minimum $\overline{MR}$	5		100	50	ns	
pulse width; HIGH	10	t_{WMRL}	40	20	ns	
	15		30	15	ns	
Recovery time	5		30	10	ns	
for $\overline{MR}$	10	t_{RMR}	15	5	ns	
	15		15	5	ns	
Maximum clock	5		5	10	MHz	
pulse frequency	10	f_{max}	14	28	MHz	
	15		19	39	MHz	

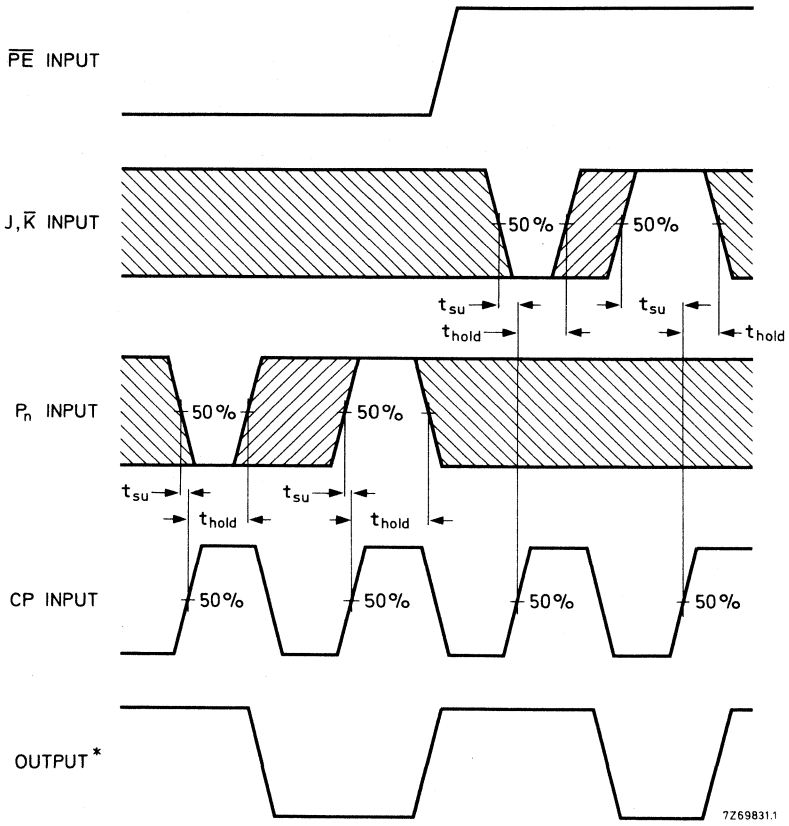
	V_{DD} V	typical formula for P (μW)	where
Dynamic power dissipation per package (P)	5	$1900\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
	10	$8300\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$22\,800\ f_i + \Sigma(f_o C_L) \times V_{DD}^2$	



Waveforms showing minimum CP pulse width and CP to output delays
Other conditions: J = $\overline{PE}$ = $\overline{MR}$ = HIGH; $\overline{K}$ = LOW

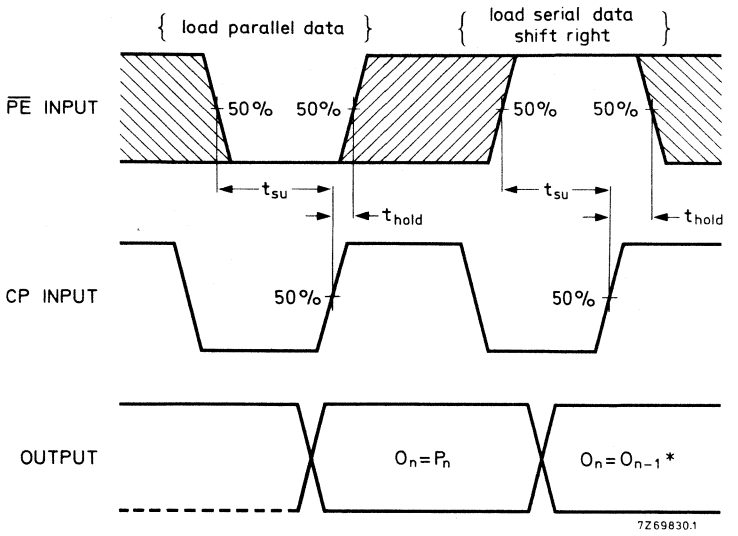


Waveforms showing minimum $\overline{MR}$ pulse width, $\overline{MR}$ to output delays and $\overline{MR}$ to CP recovery time
Other conditions: $\overline{PE}$ = LOW; $P_0 = P_1 = P_2 = P_3$ = HIGH



Waveforms showing set-up times, hold times for J, $\overline{K}$ and P_n inputs
Other conditions: $\overline{MR}$ = HIGH

* J and $\overline{K}$ set-up times affect O_0 only.



Waveforms showing set-up times and hold times for $\overline{PE}$ input
Other conditions: $\overline{MR}$ = HIGH

Note

Set-up and hold times are shown as positive values but may be specified as negative values.

* O_0 state will be determined by J and $\overline{K}$ inputs.

TYPE NUMBER DESIGNATION
ORDERING INFORMATION

TYPE NUMBER DESIGNATION

HEF4XXXBX	complete type number
HE	family identification
F	operating temperature range: −40 to + 85 °C
4XXX	device number (may be 5 digits)
B	JEDEC 'B' series C-MOS specification (UB = unbuffered)
V	reduced supply voltage range
X	package code (e.g. P = plastic; D = ceramic)

ORDERING INFORMATION

Always use the complete type number when ordering. Complete type numbers are given in the device data sheets.

HANDLING MOS DEVICES

HANDLING MOS DEVICES

Though all our MOS integrated circuits incorporate protection against electrostatic discharges, they can nevertheless be damaged by accidental over-voltages. In storing and handling them, the following precautions are recommended.

Caution

Testing or handling and mounting call for special attention to personal safety. Personnel handling MOS devices should normally be connected to ground via a resistor.

Storage and transport

Store and transport the circuits in their original packing. Alternatively, use may be made of a conductive material or special IC carrier that either short-circuits all leads or insulates them from external contact.

Testing or handling

Work on a conductive surface (e.g. metal table top) when testing the circuits or transferring them from one carrier to another. Electrically connect the person doing the testing or handling to the conductive surface, for example by a metal bracelet and a conductive cord or chain. Connect all testing and handling equipment to the same surface.
Signals should not be applied to the inputs while the device power supply is off. All unused input leads should be connected to either the supply voltage or ground.

Mounting

Mount MOS integrated circuits on printed circuit boards *after* all other components have been mounted. Take care that the circuits themselves, metal parts of the board, mounting tools, and the person doing the mounting are kept at the same electric (ground) potential. If it is impossible to ground the printed-circuit board the person mounting the circuits should touch the board before bringing MOS circuits into contact with it.

Soldering

Soldering iron tips, including those of low-voltage irons, or soldering baths should also be kept at the same potential as the MOS circuits and the board.

Static charges

Dress personnel in clothing of non-electrostatic material (no wool, silk or synthetic fibres). After the MOS circuits have been mounted on the board proper handling precautions should still be observed. Until the sub-assemblies are inserted into a complete system in which the proper voltages are supplied, the board is no more than an extension of the leads of the devices mounted on the board. To prevent static charges from being transmitted through the board wiring to the device it is recommended that conductive clips or conductive tape be put on the circuit board terminals.

Transient voltages

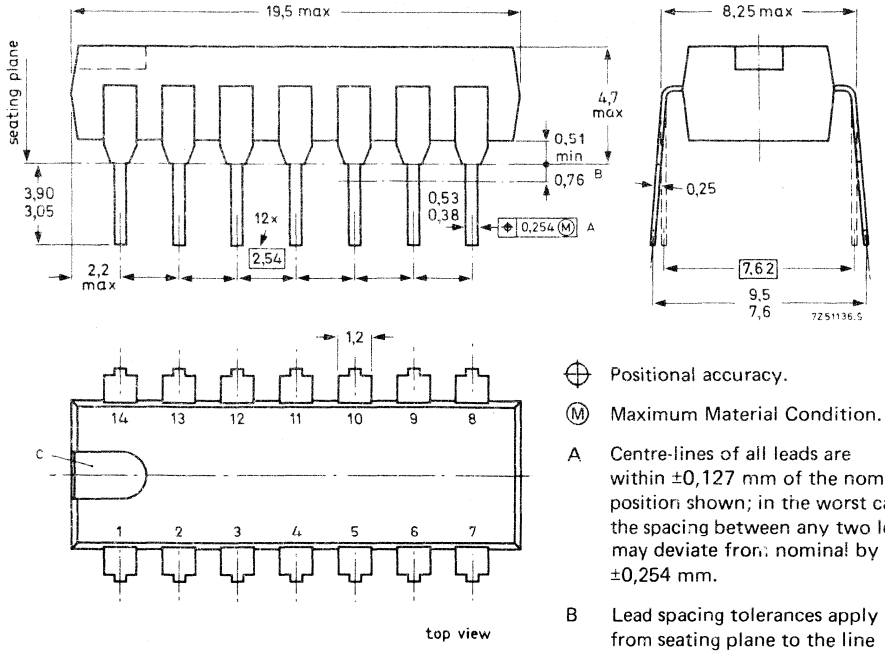
To prevent permanent damage due to transient voltages, do not insert or remove MOS devices, or printed-circuit boards with MOS devices, from test sockets or systems with power on.

Voltage surges

Beware of voltage surges due to switching electrical equipment on or off, relays and d.c. lines.

PACKAGE OUTLINES

14-LEAD DUAL IN-LINE; PLASTIC (SOT-27)



Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

C Index may be horizontal as shown, or vertical.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

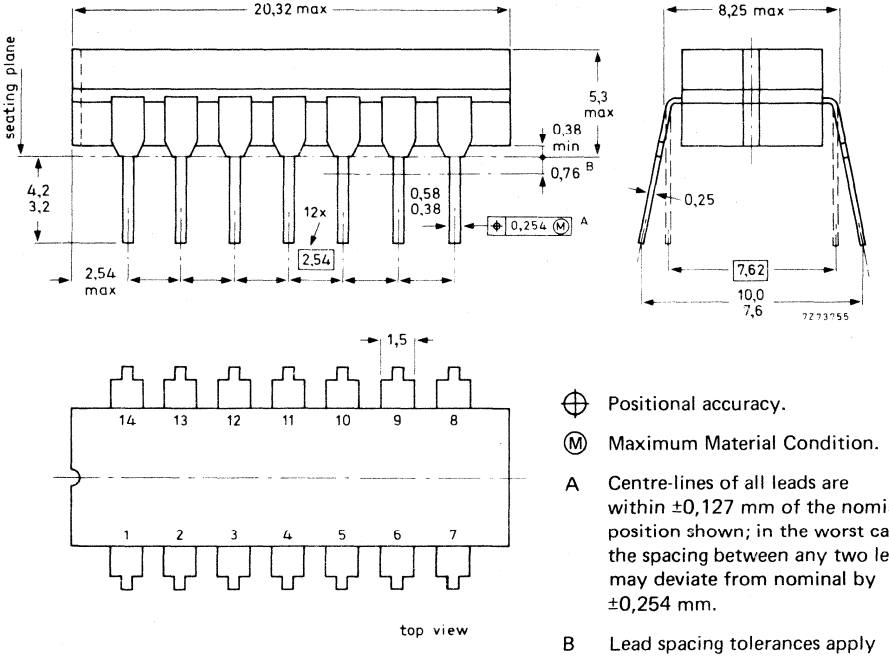
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

14-LEAD DUAL IN-LINE; CERAMIC (SOT-73)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

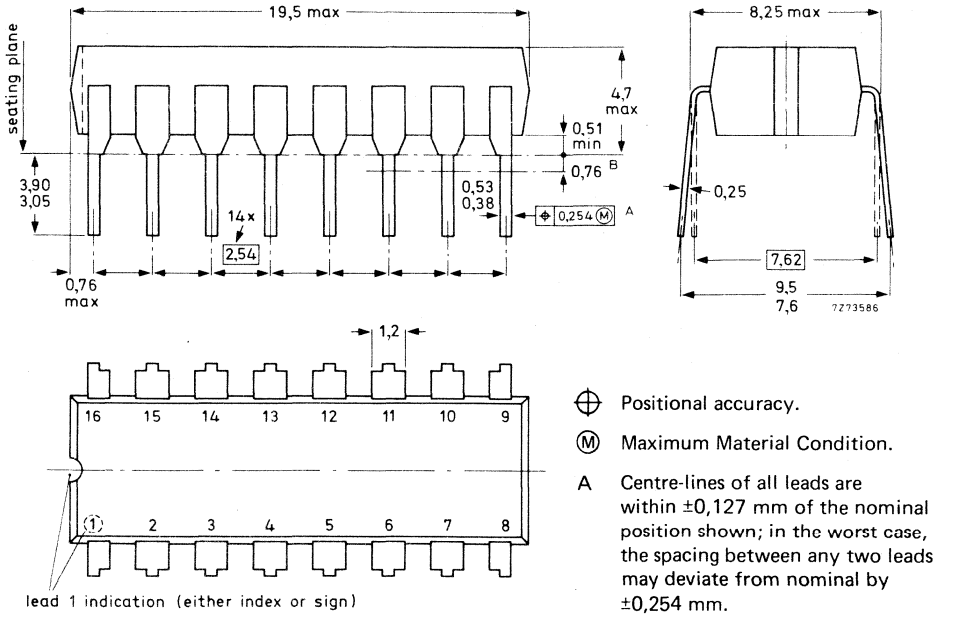
B Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

16-LEAD DUAL IN-LINE; PLASTIC (SOT-38Z)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

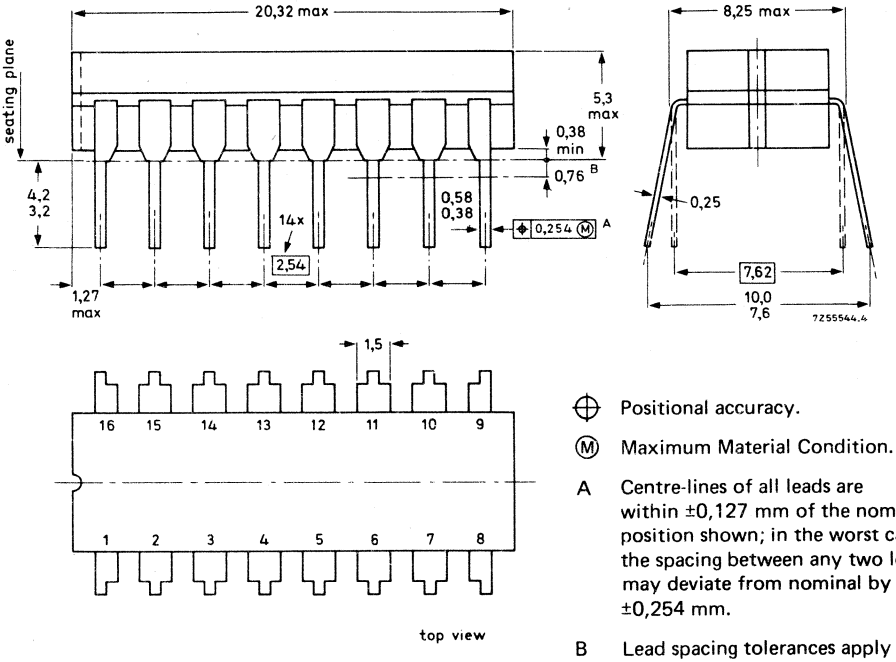
2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.

16-LEAD DUAL IN-LINE; CERAMIC (SOT-74)



⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

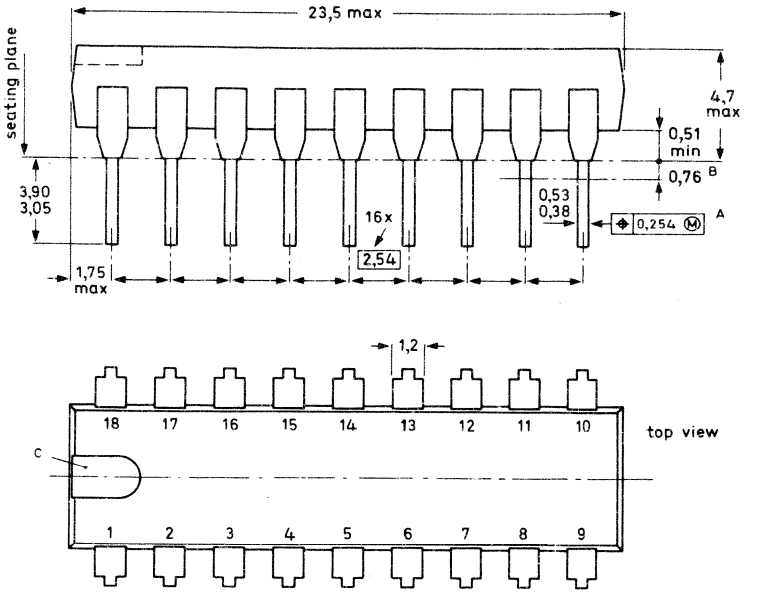
B Lead spacing tolerances apply from seating plane to the line indicated.

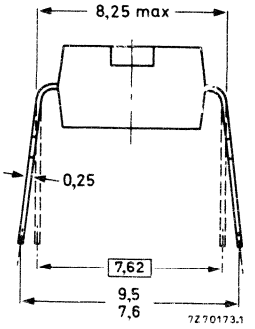
Dimensions in mm

Remarks

1. Leads are given positive misalignment so that they grip after insertion.
2. Leads are Ni-Fe, pure tin plated.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102A)





side view

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

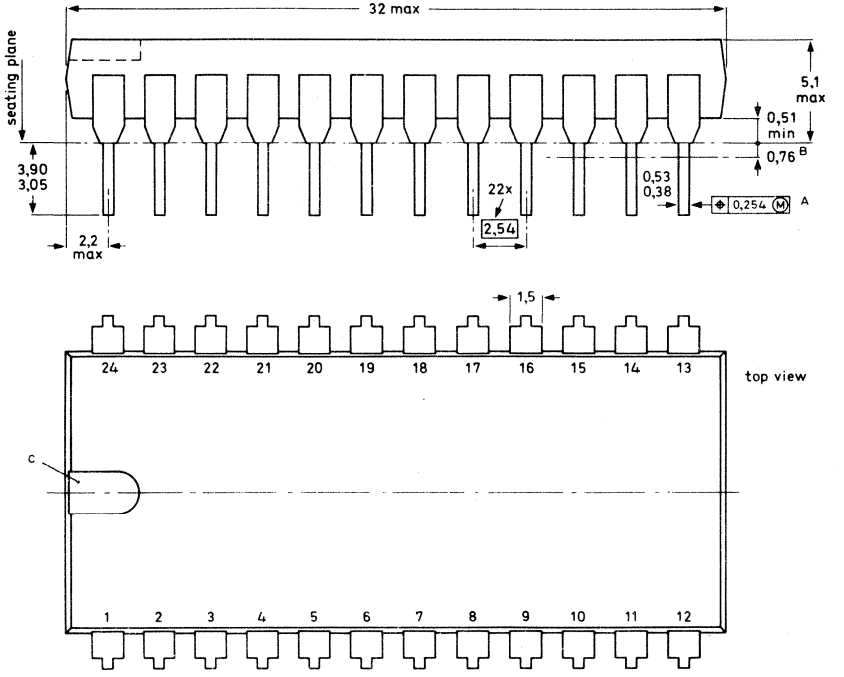
C Index may be horizontal as shown, or vertical.

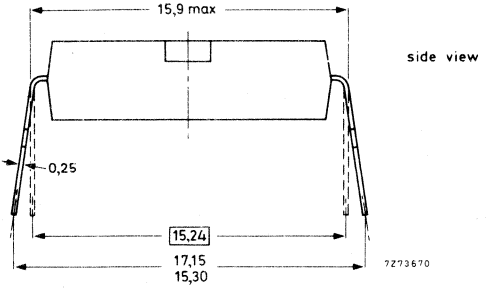
Dimensions in mm

SOLDERING

See page 1 of this chapter (SOT-27).

24-LEAD DUAL IN-LINE; PLASTIC (SOT-101A)





⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

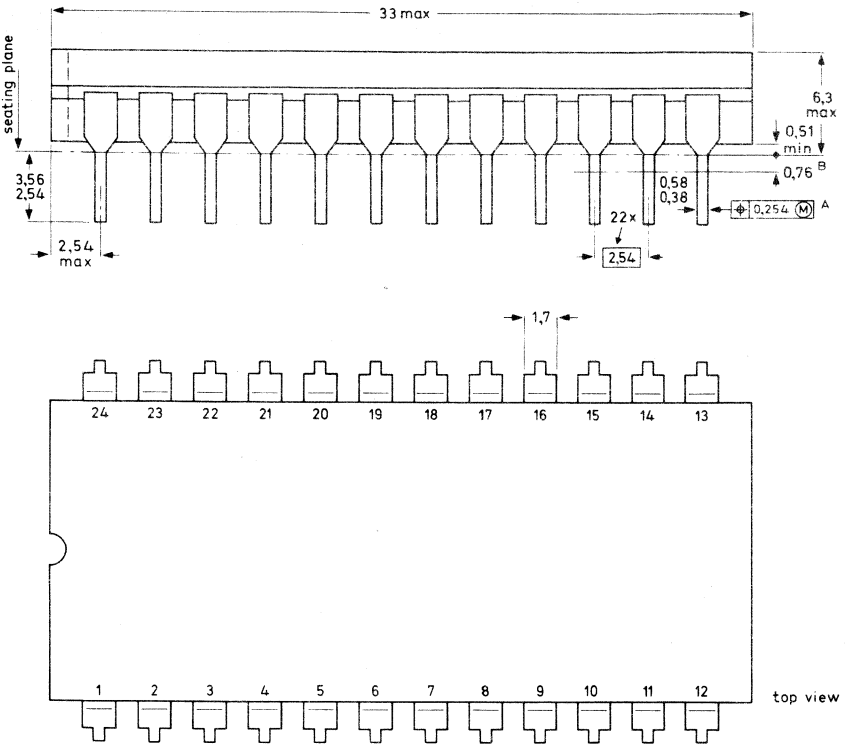
C Index may be horizontal as shown, or vertical.

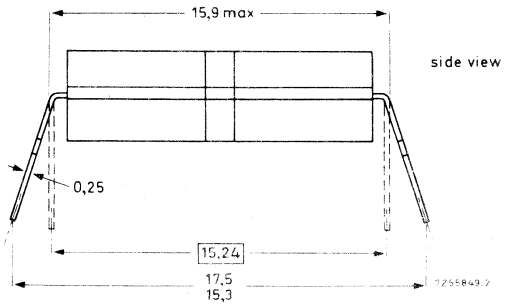
Dimensions in mm

SOLDERING

See page 1 of this chapter (SOT-27).

24-LEAD DUAL IN-LINE; CERAMIC (SOT-94)





⊕ Positional accuracy.

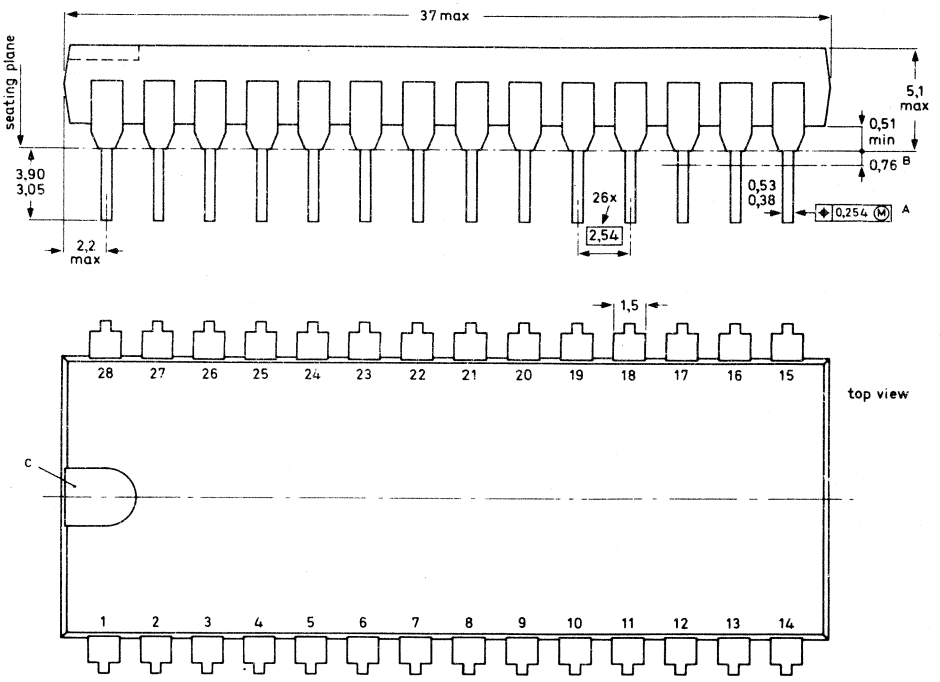
Ⓜ Maximum Material Condition.

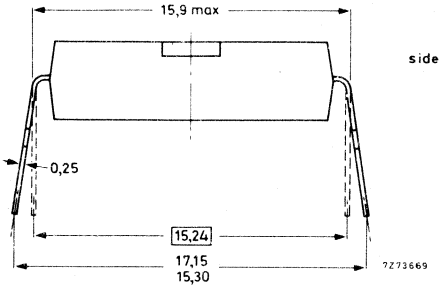
A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

B Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

28-LEAD DUAL IN-LINE; PLASTIC (SOT-117)





Dimensions in mm

⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

A Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

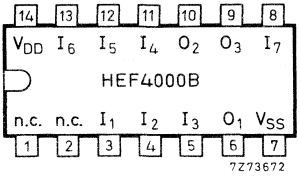
B Lead spacing tolerances apply from seating plane to the line indicated.

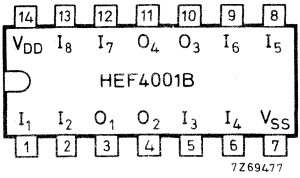
C Index may be horizontal as shown, or vertical.

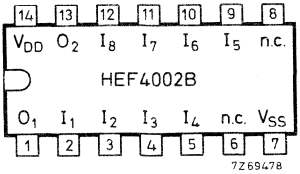
SOLDERING

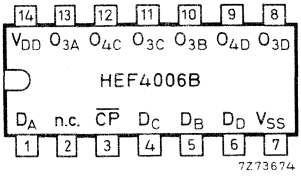
See page 1 of this chapter (SOT-27).

PIN DESIGNATIONS


14 13 12 11 10 9 8
VDD I6 I5 I4 O2 O3 I7
HEF4000B
n.c. n.c. I1 I2 I3 O1 VSS
1 2 3 4 5 6 7
7Z73672


14 13 12 11 10 9 8
VDD I8 I7 O4 O3 I6 I5
HEF4001B
I1 I2 O1 O2 I3 I4 VSS
1 2 3 4 5 6 7
7Z69477


14 13 12 11 10 9 8
VDD O2 I8 I7 I6 I5 n.c.
HEF4002B
O1 I1 I2 I3 I4 n.c. VSS
1 2 3 4 5 6 7
7Z69478


14 13 12 11 10 9 8
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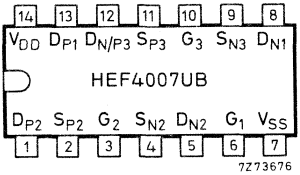
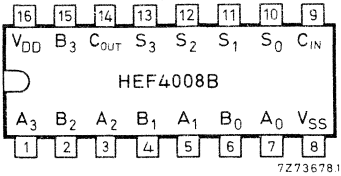
HEF4006B
DA n.c. CP DC DB DD VSS
1 2 3 4 5 6 7
7Z73674


14 13 12 11 10 9 8
VDD DP1 DN/P3 SP3 G3 SN3 DN1
HEF4007UB
DP2 SP2 G2 SN2 DN2 G1 VSS
1 2 3 4 5 6 7
7Z73676


16 15 14 13 12 11 10 9
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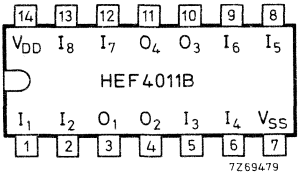
HEF4008B
A3 B2 A2 B1 A1 B0 A0 VSS
1 2 3 4 5 6 7 8
7Z73678.1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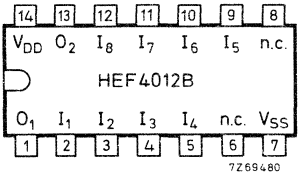
HEF4011B
I1 I2 O1 O2 I3 I4 VSS
1 2 3 4 5 6 7
7Z69479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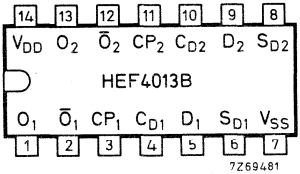
HEF4012B
O1 I1 I2 I3 I4 n.c. VSS
1 2 3 4 5 6 7
7Z69480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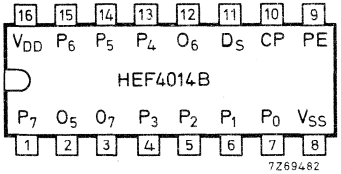
HEF4013B
O1 Ō1 CP1 CD1 D1 SD1 VSS
1 2 3 4 5 6 7
7Z69481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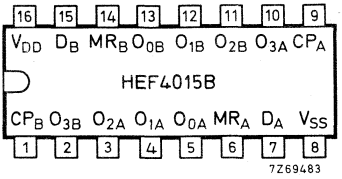
P7 O5 O7 P3 P2 P1 P0 VSS
1 2 3 4 5 6 7 8
7Z69482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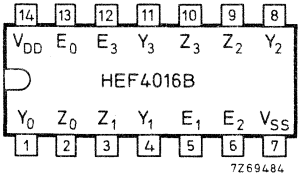
VDD DB MRB O0B O1B O2B O3A CPA
HEF4015B
CPB O3B O2A O1A O0A MRA DA VSS
1 2 3 4 5 6 7 8
7Z69483


14 13 12 11 10 9 8
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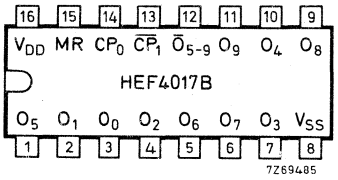
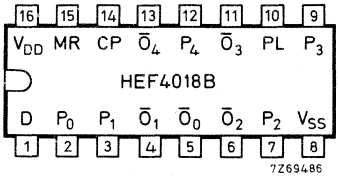
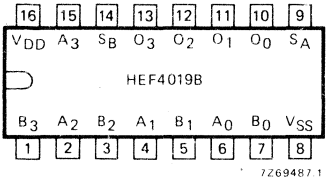
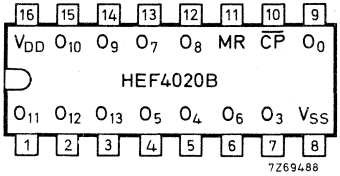
HEF4016B
Y0 Z0 Z1 Y1 E1 E2 VSS
1 2 3 4 5 6 7
7Z69484

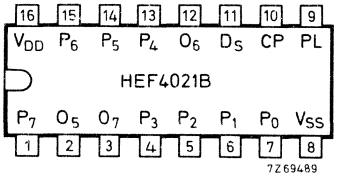
PIN DESIGNATIONS

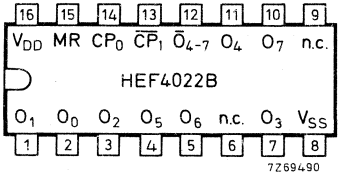


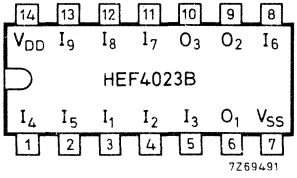


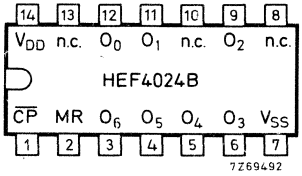


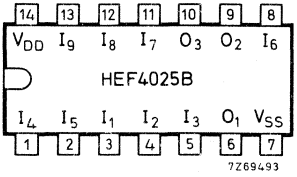


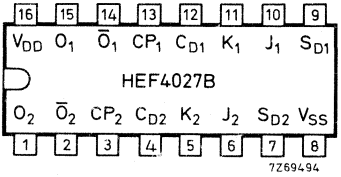


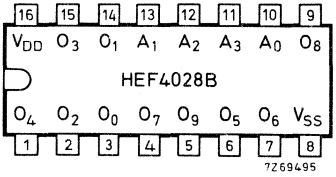


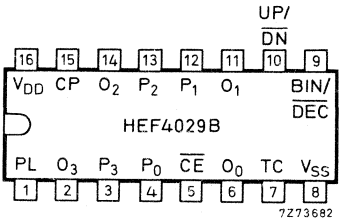


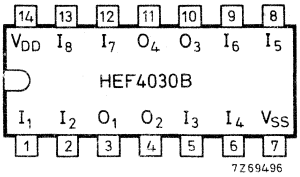








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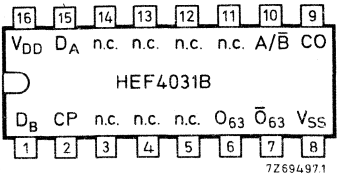
HEF4030B
I1 I2 O1 O2 I3 I4 VSS
1 2 3 4 5 6 7
7Z69496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DB CP n.c. n.c. n.c. O63 O63 VSS
1 2 3 4 5 6 7 8
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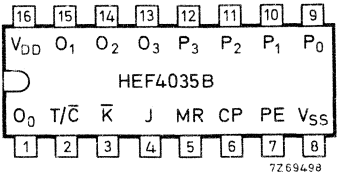
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HEF4035B
O0 T/C K J MR CP PE VSS
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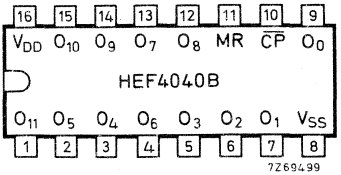
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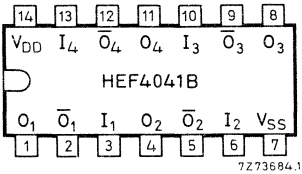
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O1 O1 I1 O2 O2 I2 VSS
1 2 3 4 5 6 7
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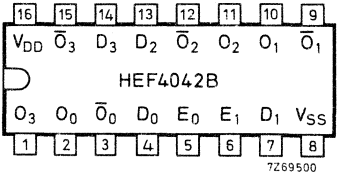
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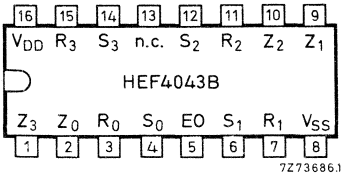
VDD O3 D3 D2 O2 O2 O1 O1
HEF4042B
O3 O0 O0 D0 E0 E1 D1 VSS
1 2 3 4 5 6 7 8
7Z69500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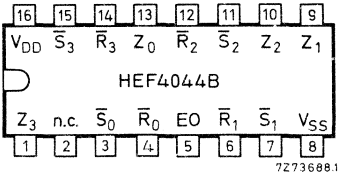
VDD R3 S3 n.c. S2 R2 Z2 Z1
HEF4043B
Z3 Z0 R0 S0 EO S1 R1 VSS
1 2 3 4 5 6 7 8
7Z73686.1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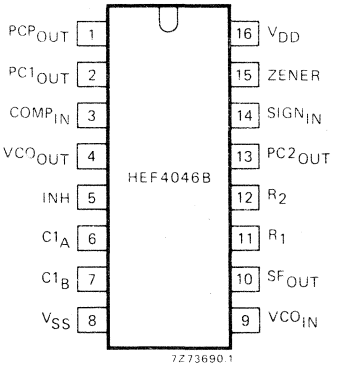
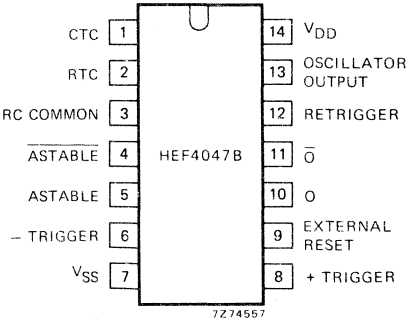
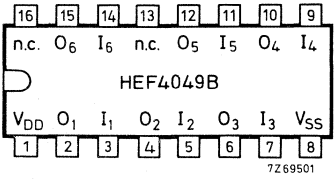
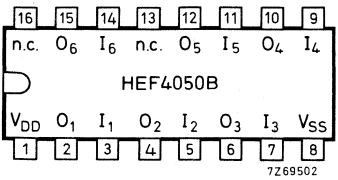
VDD S3 R3 Z0 R2 S2 Z2 Z1
HEF4044B
Z3 n.c. S0 R0 EO R1 S1 VSS
1 2 3 4 5 6 7 8
7Z73688.1

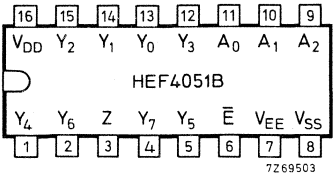

PCPOUT 1
PC1OUT 2
COMPIN 3
VCOOUT 4
INH 5
C1A 6
C1B 7
VSS 8
16 VDD
15 ZENER
14 SIGNIN
13 PC2OUT
12 R2
11 R1
10 SFOUT
9 VCOIN
HEF4046B
7Z73690.1

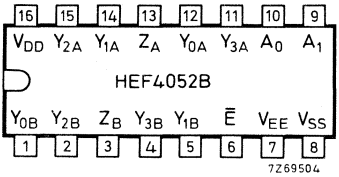

CTC 1
RTC 2
RC COMMON 3
ASTABLE 4
ASTABLE 5
– TRIGGER 6
VSS 7
14 VDD
13 OSCILLATOR OUTPUT
12 RETRIGGER
11 Q̄
10 Q
9 EXTERNAL RESET
8 + TRIGGER
HEF4047B
7Z74557

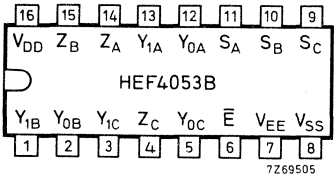
PIN DESIGNATIONS

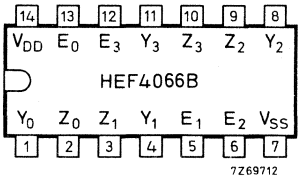


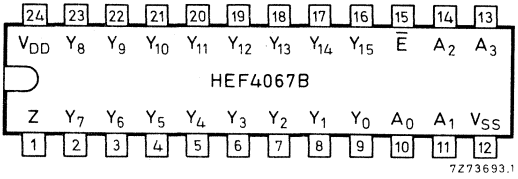


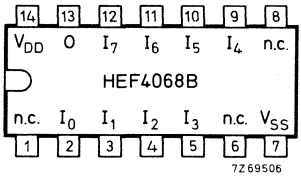


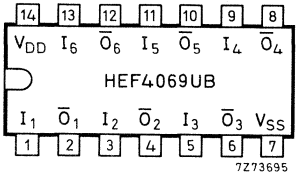


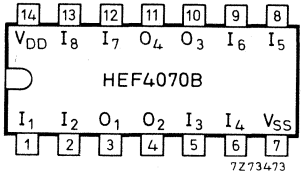


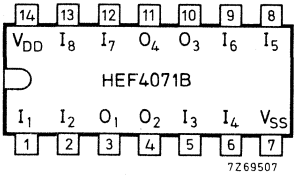


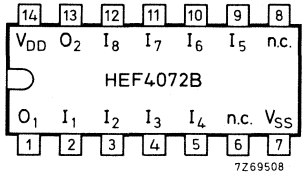


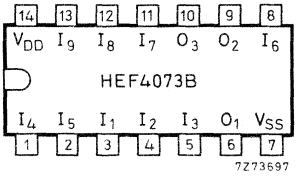








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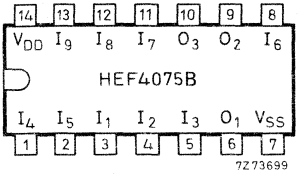
7Z73697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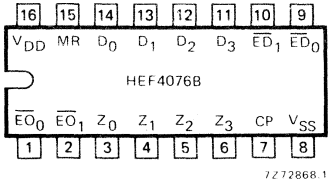
7Z73699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EO0 EO1 Z0 Z1 Z2 Z3 CP VSS
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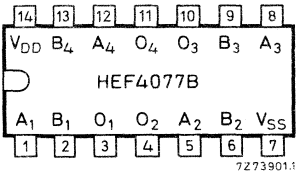
7Z72868.1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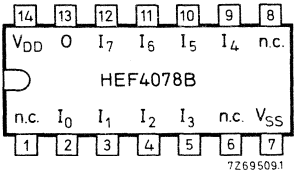
7Z73901.1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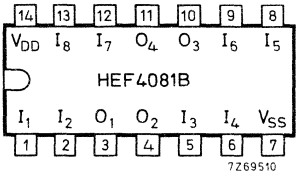
n.c. I0 I1 I2 I3 n.c. VSS
1 2 3 4 5 6 7
7Z69509.1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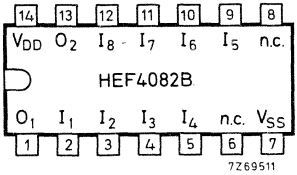
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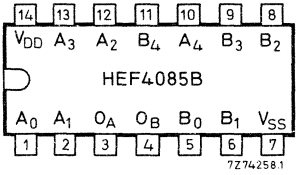
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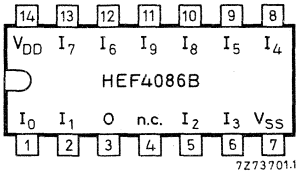
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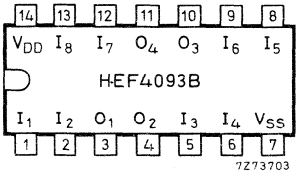
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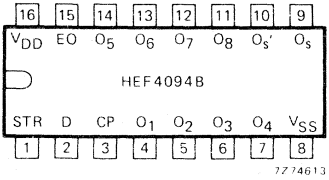
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STR D CP O1 O2 O3 O4 VSS
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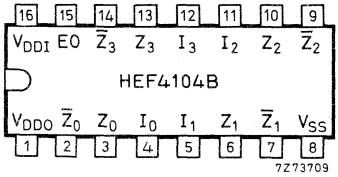
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VDDI EO Z̄3 Z3 I3 I2 Z2 Z̄2
HEF4104B
VDDO Z̄0 Z0 I0 I1 Z1 Z̄1 VSS
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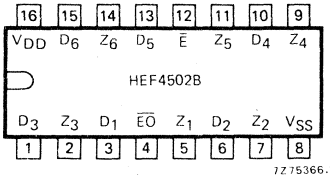
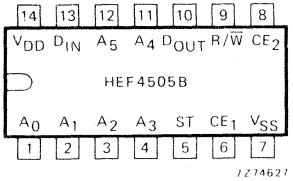
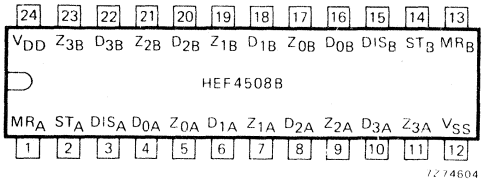
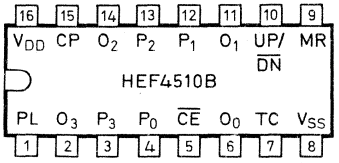
7Z73709

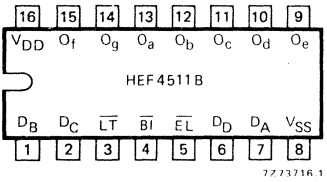
PIN DESIGNATIONS

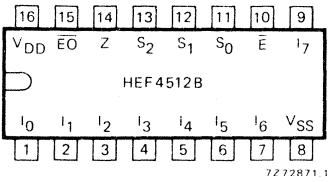


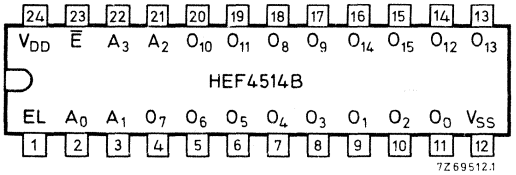


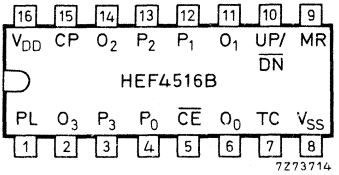


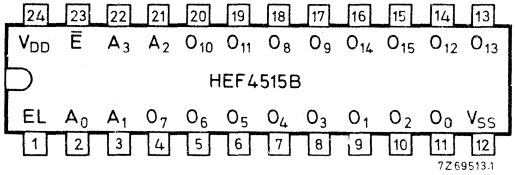


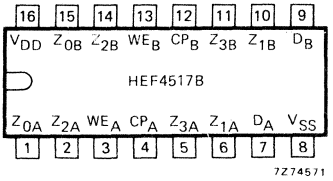


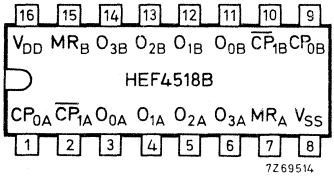


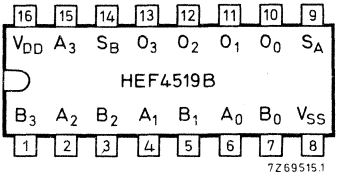


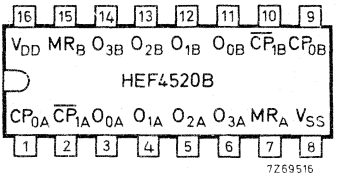


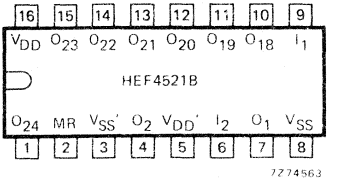


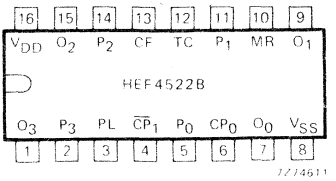


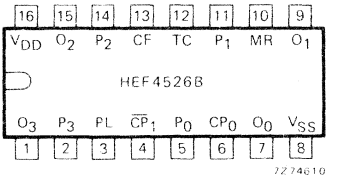





16 15 14 13 12 11 10 9
VDD MRB O3B O2B O1B O0B CP1B CP0B
HEF4520B
CP0A CP1A O0A O1A O2A O3A MRA VSS
1 2 3 4 5 6 7 8
7Z69516


16 15 14 13 12 11 10 9
VDD O23 O22 O21 O20 O19 O18 I1
HEF4521B
O24 MR VSS O2 VDD I2 O1 VSS
1 2 3 4 5 6 7 8
7Z74563


16 15 14 13 12 11 10 9
VDD O2 P2 CF TC P1 MR O1
HEF4522B
O3 P3 PL CP1 P0 CP0 O0 VSS
1 2 3 4 5 6 7 8
7Z74611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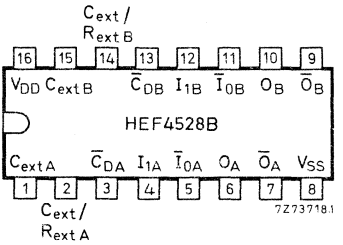
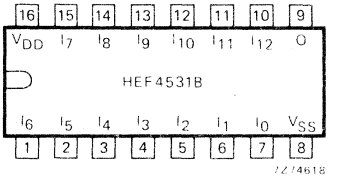
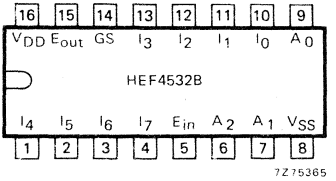
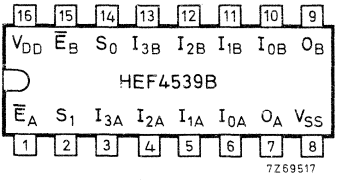
VDD O2 P2 CF TC P1 MR O1
HEF4526B
O3 P3 PL CP1 P0 CP0 O0 VSS
1 2 3 4 5 6 7 8
7Z74610

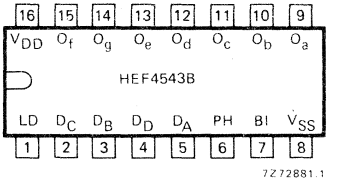

Cext / Rext B
16 15 14 13 12 11 10 9
VDD Cext B C̄DB I1B Ī0B O0B Ō0B
HEF4528B
Cext A C̄DA I1A Ī0A O0A Ō0A VSS
1 2 3 4 5 6 7 8
Cext / Rext A
7Z737181


16 15 14 13 12 11 10 9
VDD I7 I8 I9 I10 I11 I12 O
HEF4531B
I6 I5 I4 I3 I2 I1 I0 VSS
1 2 3 4 5 6 7 8
7Z74618


16 15 14 13 12 11 10 9
VDD Eout GS I3 I2 I1 I0 A0
HEF4532B
I4 I5 I6 I7 Ein A2 A1 VSS
1 2 3 4 5 6 7 8
7Z75365


24 23 22 21 20 19 18 17 16 15 14 13
VDD C̄PB Cext2 ĒZB ZB0 ZB1 ZB2 ZB3 ZS3 ĒZS ZS2 TC
HEF4534B
Cext1 MR OER CPA MA MB ZS0 ZS1 SR CPS ZS4 VSS
1 2 3 4 5 6 7 8 9 10 11 12
7Z74602


16 15 14 13 12 11 10 9
VDD Ē B S0 I3B I2B I1B I0B OB
HEF4539B
Ē A S1 I3A I2A I1A I0A OA VSS
1 2 3 4 5 6 7 8
7Z69517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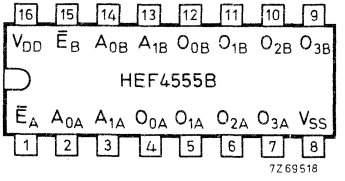
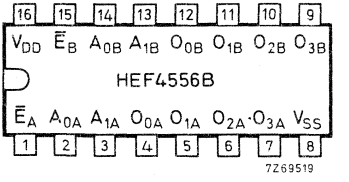
VDD Of Og Oe Od Oc Ob Oa
HEF4543B
LD DC DB DD DA PH BI VSS
1 2 3 4 5 6 7 8
7Z72881.1


16 15 14 13 12 11 10 9
VDD Ē B A0B A1B O0B O1B O2B O3B
HEF4555B
Ē A A0A A1A O0A O1A O2A O3A VSS
1 2 3 4 5 6 7 8
7Z69518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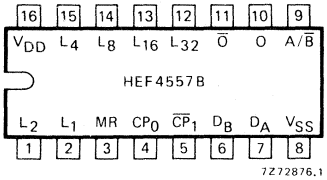
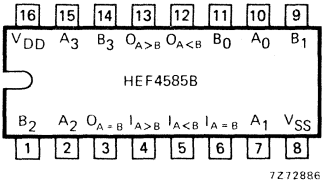
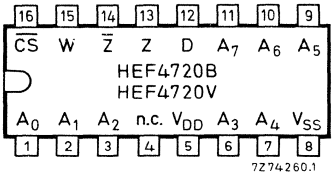
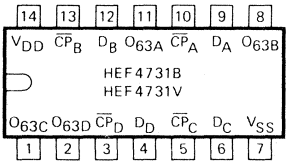
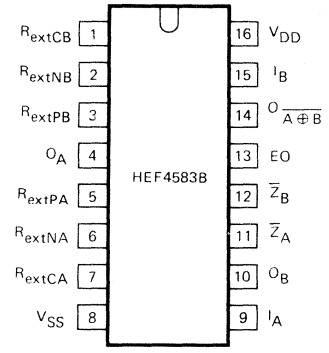
VDD Ē B A0B A1B O0B O1B O2B O3B
HEF4556B
Ē A A0A A1A O0A O1A O2A·O3A VSS
1 2 3 4 5 6 7 8
7Z69519

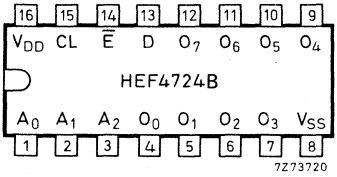

16 15 14 13 12 11 10 9
VDD L4 L8 L16 L32 Ō O A/B
HEF4557B
L2 L1 MR CP0 CP1 DB DA VSS
1 2 3 4 5 6 7 8
7Z72876.1

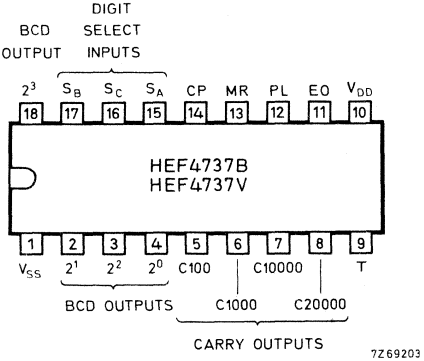

16 15 14 13 12 11 10 9
VDD A3 B3 OA>B OA<B B0 A0 B1
HEF4585B
B2 A2 OA=B IA>B IA<B IA=B A1 VSS
1 2 3 4 5 6 7 8
7Z72886

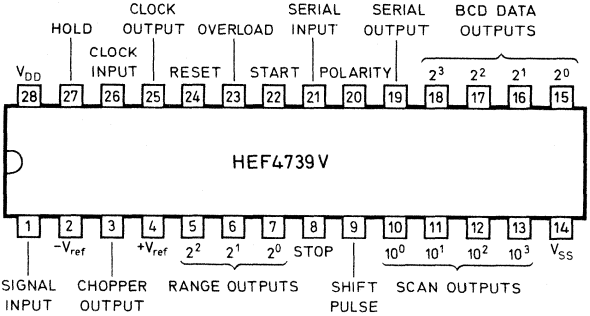

16 15 14 13 12 11 10 9
CS W Z Z D A7 A6 A5
HEF4720B
HEF4720V
A0 A1 A2 n.c. VDD A3 A4 VSS
1 2 3 4 5 6 7 8
7Z74260.1

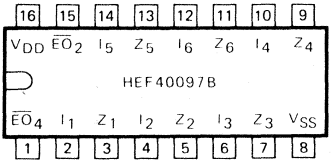

14 13 12 11 10 9 8
VDD CPB DB O63A CPA DA O63B
HEF4731B
HEF4731V
O63C O63D CPD DD CPC DC VSS
1 2 3 4 5 6 7
7Z74631

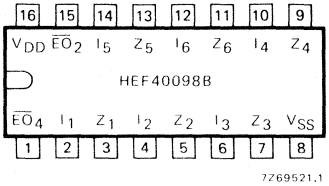

RextCB 1
RextNB 2
RextPB 3
OA 4
RextPA 5
RextNA 6
RextCA 7
VSS 8
HEF4583B
16 VDD
15 IB
14 O A⊕B
13 EO
12 Z̄B
11 Z̄A
10 OB
9 IA
7Z74621

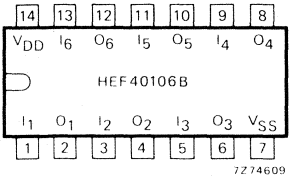

16 15 14 13 12 11 10 9
VDD CL Ē D O7 O6 O5 O4
HEF4724B
A0 A1 A2 O0 O1 O2 O3 VSS
1 2 3 4 5 6 7 8
7Z73720


BCD OUTPUT
DIGIT SELECT INPUTS
2³ SB SC SA CP MR PL EO VDD
18 17 16 15 14 13 12 11 10
HEF4737B
HEF4737V
1 2 3 4 5 6 7 8 9
VSS 2¹ 2² 2⁰ C100 C10000 T
BCD OUTPUTS
C1000 C20000
CARRY OUTPUTS
7Z69203


HOLD
CLOCK INPUT
CLOCK OUTPUT
OVERLOAD
RESET
START
SERIAL INPUT
POLARITY
SERIAL OUTPUT
BCD DATA OUTPUTS
VDD 28 27 26 25 24 23 22 21 20 19 18 17 16 15
2³ 2² 2¹ 2⁰
HEF4739V
1 2 3 4 5 6 7 8 9 10 11 12 13 14
SIGNAL INPUT
CHOPPER OUTPUT
-Vref
+Vref
2² 2¹ 2⁰ STOP
RANGE OUTPUTS
SHIFT PULSE
10⁰ 10¹ 10² 10³
SCAN OUTPUTS
VSS
7Z72116.3


16 15 14 13 12 11 10 9
VDD EO2 I5 Z5 I6 Z6 I4 Z4
HEF40097B
EO4 I1 Z1 I2 Z2 I3 Z3 VSS
1 2 3 4 5 6 7 8
7Z69520.1


16 15 14 13 12 11 10 9
VDD EO2 I5 Z5 I6 Z6 I4 Z4
HEF40098B
EO4 I1 Z1 I2 Z2 I3 Z3 VSS
1 2 3 4 5 6 7 8
7Z69521.1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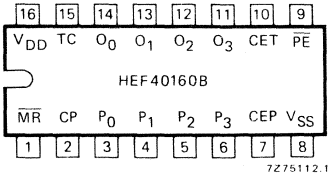
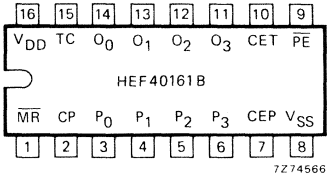
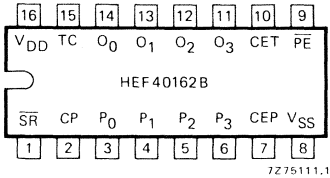
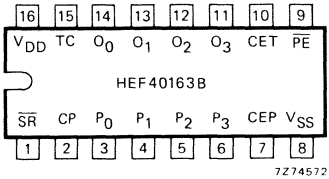
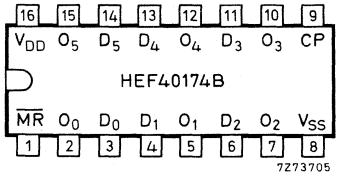
VDD I6 O6 I5 O5 I4 O4
HEF40106B
I1 O1 I2 O2 I3 O3 VSS
1 2 3 4 5 6 7
7Z74609

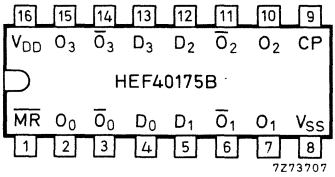

16 15 14 13 12 11 10 9
VDD TC O0 O1 O2 O3 CET PE
HEF40160B
MR CP P0 P1 P2 P3 CEP VSS
1 2 3 4 5 6 7 8
7Z75112.1


16 15 14 13 12 11 10 9
VDD TC O0 O1 O2 O3 CET PE
HEF40161B
MR CP P0 P1 P2 P3 CEP VSS
1 2 3 4 5 6 7 8
7Z74566


16 15 14 13 12 11 10 9
VDD TC O0 O1 O2 O3 CET PE
HEF40162B
SR CP P0 P1 P2 P3 CEP VSS
1 2 3 4 5 6 7 8
7Z75111.1


16 15 14 13 12 11 10 9
VDD TC O0 O1 O2 O3 CET PE
HEF40163B
SR CP P0 P1 P2 P3 CEP VSS
1 2 3 4 5 6 7 8
7Z74572


16 15 14 13 12 11 10 9
VDD O5 D5 D4 O4 D3 O3 CP
HEF40174B
MR O0 D0 D1 O1 D2 O2 VSS
1 2 3 4 5 6 7 8
7Z73705


16 15 14 13 12 11 10 9
VDD O3 O3 D3 D2 O2 O2 CP
HEF40175B
MR O0 O0 D0 D1 O1 O1 VSS
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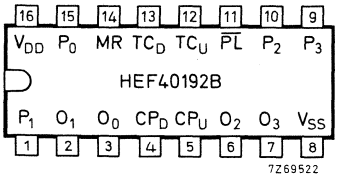
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P1 O1 O0 CPD CPU O2 O3 VSS
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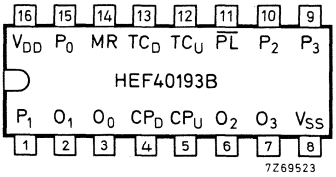
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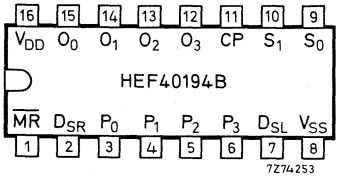
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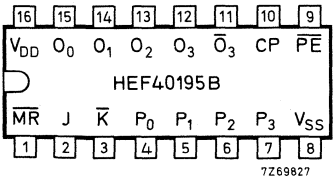
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MR J K P0 P1 P2 P3 VSS
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7Z69827

FUNCTIONAL AND NUMERICAL INDEX

NAND gates	HEF4011B	quadruple 2-input NAND gate
	HEF4012B	dual 4-input NAND gate
	HEF4023B	triple 3-input NAND gate
	HEF4068B	8-input NAND gate
AND gates	HEF4073B	triple 3-input AND gate
	HEF4081B	quadruple 2-input AND gate
	HEF4082B	dual 4-input AND gate
NOR gates	HEF4000B	dual 3-input NOR gate and inverter
	HEF4001B	quadruple 2-input NOR gate
	HEF4002B	dual 4-input NOR gate
	HEF4025B	triple 3-input NOR gate
	HEF4078B	8-input NOR gate
OR gates	HEF4071B	quadruple 2-input OR gate
	HEF4072B	dual 4-input OR gate
	HEF4075B	triple 3-input OR gate
Inverters and buffers	HEF4007UB	dual complementary pair and inverter
	HEF4041B	quadruple true/complement buffer
	HEF4049B	hex inverting buffers
	HEF4050B	hex non-inverting buffers
	HEF4069UB	hex inverter
	HEF4502B	strobed hex inverter/buffer
	HEF40097B	3-state hex non-inverting buffer
	HEF40098B	3-state hex inverting buffer
Complex gates	HEF4030B	quadruple EXCLUSIVE-OR gate
	HEF4070B	quadruple EXCLUSIVE-OR gate
	HEF4077B	quadruple EXCLUSIVE-NOR gate
	HEF4085B	dual 2-wide 2-input AND-OR-invert gate
	HEF4086B	4-wide 2-input AND-OR-invert gate
Flip-flops	HEF4013B	dual D-type flip-flop
	HEF4027B	dual JK flip-flop
	HEF4076B	quadruple D-type register with 3-state outputs
	HEF40174B	hex D-type flip-flop
	HEF40175B	quadruple D-type flip-flop
Counters	HEF4017B	5-stage Johnson counter
	HEF4018B	presettable divide-by-n counter
	HEF4020B	14-stage binary counter
	HEF4022B	4-stage divide-by-8 Johnson counter
	HEF4024B	7-stage binary counter
	HEF4029B	synchronous up/down counter, binary/decade counter
	HEF4040B	12-stage binary counter
	HEF4510B	BCD up/down counter
	HEF4516B	binary up/down counter
	HEF4518B	dual BCD counter
	HEF4520B	dual binary counter

Counters (continued)	HEF4521B	24-stage frequency divider
	HEF4522B	programmable 4-bit BCD down counter
	HEF4526B	programmable 4-bit binary down counter
	HEF4534B	real time 5-decade counter
	HEF4737B; V	quadruple static decade counters
	HEF40160B	4-bit synchronous decade counter with asynchronous reset
	HEF40161B	4-bit synchronous binary counter with asynchronous reset
	HEF40162B	4-bit synchronous decade counter with synchronous reset
	HEF40163B	4-bit synchronous binary counter with synchronous reset
	HEF40192B	4-bit up/down decade counter
	HEF40193B	4-bit up/down binary counter
Registers	HEF4006B	18-stage static shift register
	HEF4014B	8-bit shift register
	HEF4015B	dual 4-bit static shift register
	HEF4021B	8-bit static shift register
	HEF4031B	64-state static shift register
	HEF4035B	4-bit universal shift register
	HEF4076B	quadruple D-type register with 3-state outputs
	HEF4094B	8-stage shift-and-store bus register
	HEF4517B	dual 64-bit static shift register
	HEF4557B	1-to-64 bit variable length shift register
	HEF4731B; V	quadruple 64-bit static shift register
	HEF40194B	4-bit bidirectional universal shift register
	HEF40195B	4-bit universal shift register
Decoders	HEF4028B	1-of-10 decoder
	HEF4511B	BCD to 7-segment latch/decoder/driver
	HEF4514B	1-of-16 decoder/demultiplexer with input latches
	HEF4515B	1-of-16 decoder/demultiplexer with input latches
	HEF4543B	BCD to 7-segment latch/decoder/driver
	HEF4555B	dual 1-of-4 decoder/demultiplexer
	HEF4556B	dual 1-of-4 decoder/demultiplexer
Digital multiplexers	HEF4019B	quadruple 2-input multiplexer
	HEF4512B	8-input multiplexer with 3-state output
	HEF4519B	quadruple 2-input multiplexer
	HEF4539B	dual 4-input multiplexer
Analogue switches and multiplexers/demultiplexers	HEF4016B	quadruple bilateral switches
	HEF4051B	8-channel analogue multiplexer/demultiplexer
	HEF4052B	dual 4-channel analogue multiplexer/demultiplexer
	HEF4053B	triple 2-channel analogue multiplexer/demultiplexer
	HEF4066B	quadruple bilateral switches
	HEF4067B	16-channel analogue multiplexer/demultiplexer

Latches	HEF4042B	quadruple D-latch
	HEF4043B	quadruple R/S latch with 3-state outputs
	HEF4044B	quadruple R/S latch with 3-state outputs
	HEF4508B	dual 4-bit latch
	HEF4724B	8-bit addressable latch
Translator	HEF4104B	quadruple low to high voltage translator with 3-state outputs
Memories	HEF4505B	64-bit, 1-bit per word read/write RAM
	HEF4720B; V	256-bit, 1-bit per word RAM
Multivibrators	HEF4047B	monostable/astable multivibrator
	HEF4528B	dual monostable multivibrator
Arithmetic circuits	HEF4008B	4-bit binary full adder
	HEF4531B	13-input parity checker/generator
	HEF4532B	8-input priority encoder
	HEF4585B	4-bit magnitude comparator
Schmitt triggers	HEF4093B	quadruple 2-input NAND Schmitt trigger
	HEF4583B	dual Schmitt trigger
	HEF40106B	hex Schmitt trigger
Specials	HEF4046B	phase-locked loop
	HEF4739V	digital voltmeter circuit

NUMERICAL INDEX

type number	function	category	pins	suffix *
HEF4000B	dual 3-input NOR gate and inverter	gates	14	D, P
HEF4001B	quadruple 2-input NOR gate	gates	14	D, P
HEF4002B	dual 4-input NOR gate	gates	14	D, P
HEF4006B	18-stage static shift register	MSI	14	D, P
HEF4007UB	dual complementary pair and inverter	gates	14	D, P
HEF4008B	4-bit binary full adder	MSI	16	D, P
HEF4011B	quadruple 2-input NAND gate	gates	14	D, P
HEF4012B	dual 4-input NAND gate	gates	14	D, P
HEF4013B	dual D-type flip-flop	flip-flops	14	D, P
HEF4014B	8-bit shift register	MSI	16	D, P
HEF4015B	dual 4-bit static shift register	MSI	16	D, P
HEF4016B	quadruple bilateral switches	gates	16	D, P
HEF4017B	5-stage Johnson counter	MSI	16	D, P
HEF4018B	presettable divide-by-n counter	MSI	16	D, P
HEF4019B	quadruple 2-input multiplexer	MSI	16	D, P
HEF4020B	14-stage binary counter	MSI	16	D, P
HEF4021B	8-bit static shift register	MSI	16	D, P
HEF4022B	4-stage divide-by-8 Johnson counter	MSI	16	D, P
HEF4023B	triple 3-input NAND gate	gates	14	D, P
HEF4024B	7-stage binary counter	MSI	14	D, P
HEF4025B	triple 3-input NOR gate	gates	14	D, P
HEF4027B	dual JK flip-flop	flip-flops	16	D, P
HEF4028B	1-of-10 decoder	MSI	16	D, P
HEF4029B	synchronous up/down - binary/decade counter	MSI	16	D, P
HEF4030B	quadruple EXCLUSIVE-OR gate	gates	14	D, P
HEF4031B	64-state static shift register	LSI	16	D, P
HEF4035B	4-bit universal shift register	MSI	16	D, P
HEF4040B	12-stage binary counter	MSI	16	D, P
HEF4041B	quadruple true/complement buffer	buffers	14	D, P
HEF4042B	quadruple D-latch	MSI	16	D, P
HEF4043B	quadruple R/S latch with 3-state outputs	MSI	16	D, P
HEF4044B	quadruple R/S latch with 3-state outputs	MSI	16	D, P
HEF4046B	phase-locked loop	MSI	16	D, P
HEF4047B	monostable/astable multivibrator	MSI	14	D, P
HEF4049B	hex inverting buffers	buffers	16	D, P

* Add the suffix to the type number on all orders.
D ceramic package.
P plastic package.

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type number	function	category	pins	suffix *
HEF4050B	hex non-inverting buffers	buffers	16	D, P
HEF4051B	8-channel analogue multiplexer/demultiplexer	MSI	16	D, P
HEF4052B	dual 4-channel analogue multiplexer/demultiplexer	MSI	16	D, P
HEF4053B	triple 2-channel analogue multiplexer/demultiplexer	MSI	16	D, P
HEF4066B	quadruple bilateral switches	gates	14	D, P
HEF4067B	16-channel analogue multiplexer/demultiplexer	MSI	24	D, P
HEF4068B	8-input NAND gate	gates	14	D, P
HEF4069UB	hex inverter	gates	14	D, P
HEF4070B	quadruple EXCLUSIVE-OR gate	gates	14	D, P
HEF4071B	quadruple 2-input OR gate	gates	14	D, P
HEF4072B	dual 4-input OR gate	gates	14	D, P
HEF4073B	triple 3-input AND gate	gates	14	D, P
HEF4075B	triple 3-input OR gate	gates	14	D, P
HEF4076B	quadruple D-type register with 3-state outputs	MSI	16	D, P
HEF4077B	quadruple EXCLUSIVE-NOR gate	gates	14	D, P
HEF4078B	8-input NOR gate	gates	14	D, P
HEF4081B	quadruple 2-input AND gate	gates	14	D, P
HEF4082B	dual 4-input AND gate	gates	14	D, P
HEF4085B	dual 2-wide 2-input AND-OR-invert gate	gates	14	D, P
HEF4086B	4-wide 2-input AND-OR-invert gate	gates	14	D, P
HEF4093B	quadruple 2-input NAND Schmitt trigger	gates	14	D, P
HEF4094B	8-stage shift-and-store bus register	MSI	16	D, P
HEF4104B	quadruple low to high voltage translator	MSI	16	D, P
HEF4502B	strobed hex inverter/buffer	buffers	16	D, P
HEF4505B	64-bit static read/write RAM	LSI	14	D, P
HEF4508B	dual 4-bit latch	MSI	24	D, P
HEF4510B	BCD up/down counter	MSI	16	D, P
HEF4511B	BCD to 7-segment latch/decoder/driver	MSI	16	D, P
HEF4512B	8-input multiplexer with 3-state output	MSI	16	D, P
HEF4514B	1-of-16 decoder/demultiplexer with input latches	MSI	24	D, P
HEF4515B	1-of-16 decoder/demultiplexer with input latches	MSI	24	D, P
HEF4516B	binary up/down counter	MSI	16	D, P
HEF4517B	dual 64-bit static shift register	LSI	16	D, P
HEF4518B	dual BCD counter	MSI	16	D, P
HEF4519B	quadruple 2-input multiplexer	MSI	16	D, P
HEF4520B	dual binary counter	MSI	16	D, P
HEF4521B	24-stage frequency divider	MSI	16	D, P
HEF4522B	programmable 4-bit BCD down counter	MSI	16	D, P
HEF4526B	programmable 4-bit binary down counter	MSI	16	D, P
HEF4528B	dual monostable multivibrator	MSI	16	D, P

* Add the suffix to the type number on all orders.
D ceramic package.
P plastic package.

type number	function	category	pins	suffix *
HEF4531B	13-input parity checker/generator	MSI	16	D, P
HEF4532B	8-input priority encoder	MSI	16	D, P
HEF4534B	real time 5-decade counter	LSI	24	D, P
HEF4539B	dual 4-input multiplexer	MSI	16	D, P
HEF4543B	BCD to 7-segment latch/decoder/driver	MSI	16	D, P
HEF4555B	dual 1-of-4 decoder/demultiplexer	MSI	16	D, P
HEF4556B	dual 1-of-4 decoder/demultiplexer	MSI	16	D, P
HEF4557B	1-to-64 bit variable length shift register	LSI	16	D, P
HEF4583B	dual Schmitt trigger	gates	16	D, P
HEF4585B	4-bit magnitude comparator	MSI	16	D, P
HEF4720B;V	256-bit, 1-bit per word RAM	LSI	16	D, P
HEF4724B	8-bit addressable latch	MSI	16	D, P
HEF4731B;V	quadruple 64-bit static shift register	LSI	14	D, P
HEF4737B;V	quadruple static decade counters	LSI	18	P
HEF4739V	digital voltmeter circuit	LSI	28	P
HEF40097B	3-state hex non-inverting buffer	buffers	16	D, P
HEF40098B	3-state hex inverting buffer	buffers	16	D, P
HEF40106B	hex Schmitt trigger	gates	14	D, P
HEF40160B	4-bit synchronous decade counter with asynchronous reset	MSI	16	D, P
HEF40161B	4-bit synchronous binary counter with asynchronous reset	MSI	16	D, P
HEF40162B	4-bit synchronous decade counter with synchronous reset	MSI	16	D, P
HEF40163B	4-bit synchronous binary counter with synchronous reset	MSI	16	D, P
HEF40174B	hex D-type flip-flop	MSI	16	D, P
HEF40175B	quadruple D-type flip-flop	MSI	16	D, P
HEF40192B	4-bit up/down decade counter	MSI	16	D, P
HEF40193B	4-bit up/down binary counter	MSI	16	D, P
HEF40194B	4-bit bidirectional universal shift register	MSI	16	D, P
HEF40195B	4-bit universal shift register	MSI	16	D, P

* Add the suffix to the type number on all orders.
D ceramic package.
P plastic package.

DIGITAL INTEGRATED CIRCUITS — LOCMOS

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